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A PARTICLE SWARM OPTIMIZATION APPROACH FOR LOW POWER VERY LARGE SCALE INTEGRATION ROUTING

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ABSTRACT

This study deals with the particle swarm optimization approach for optimal power dissipation in VLSI interconnect driven routing technique. Interconnect power dissipation is a major challenging research problem in Deep Submicron (DSM) regime that affects the overall circuit performance. The Buffer Insertion Buffer Sizing and Wire Sizing (BISWS) is considered for minimizing the power dissipation in VLSI circuits using interconnect wires. The shortest path constraints, buffer insert constraints and wire size constraints are used to analysis the power consumption considered for analysis. The closed form expressions for optimal power allocation is also derived. These expressions can be used to estimate the power dissipation efficiently in the physical design stages of the VLSI. It is observed that the power dissipation is optimal using the shortest path between source to sink. A novel optimization algorithm is introduced to model delay and bandwidth analytically derived and analyzed. The proposed optimization algorithm is analyzed and compared for 65, 45 and 32 nm CMOS technologies.

Keywords: Power Dissipation, Buffer Insertion, Wire Size, Shortest Path, VLSI Routing

1. INTRODUCTION

In Very Large Scale Integration (VLSI) design, interconnect delay affects the circuit performance and complexity (Tang *et al*., 2001). In Deep Submicron and Nanometer design, interconnect has become dominating factor in circuit performance and reliability. Thus the performance of the VLSI circuit is very much depends on wire routing and buffer insertion along the path.

The techniques for interconnect delay such as wire sizing, buffer insertion and buffer sizing are used. Dong *et al*. (2009) have introduced a heuristic method to solve buffer insertion and wire sizing problem. However, this method did not handle routing with obstacles. Without using any optimization technique or algorithm, the mathematical equation become complexe and number of parameters will be used to solve this routing problem. To solve this complex problem, Particle Swarm Optimization (PSO) is an optimization technique which is an evolutionary computational technique developed (Engelbrecht, 2005). PSO is a robust optimization technique based on movement and intelligent of swarm. Ayob *et al*. (2010; 2012) employed Particle Swarm Optimization (PSO) to solve buffer insertion problem in VLSI routing, with considerations on wire and buffer obstacles.

PSO approach in VLSI routing was first implemented by the authors (Dong *et al*., 2009). The algorithm was targeting to have shortest path in MRST problem. The problem does not include any buffer and obstacle in VLSI grid graph. The problem is to obtain the optimal path having the minimum value of interconnect delay from source to sink in VLSI using Grid Graph model. The routing path is obtained and then the buffer is inserted to minimize the delay. This technique will have the path with the

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shortest distance from source to sink whereas the shortest path is considered to have minimum delay. Mahanthi and Rao (2013) have introdued a stochastic based Particle Swarm Optimization algorithm is used to optimize buffer locations to find the shortest path and also simultaneously minimize the congestion.

The objective of this study is to study the impact of pre detective technology model library functions using standard nanometer specifications for efficient routing technique. The particle swarm optimization algorithm is used for optimizing the link between source and sink. The manhattan bending is used for optimizing this algorithm is incorporated. The shortest path routing is established between the source and sink. Buffers are appropriately inserted using PSO algorithm by implementing the shortest path routing in a source to sink. This proposed algorithm is useful for finding the minimum power dissipation of buffers inserted in a VLSI routing. The closed form expression for power dissipation is derived and is simulated with numerical results.

This study is organized as follows. Section II presents the proposed method for inter connect driven routing. Section III analyzes the performance of the proposed model using PSO algorithm. Simulation results are discussed in section IV and section V concludes the study.

2. MATERIALS AND METHODS

2.1. Power Dissipation

The interconnect width and spacing are optimized unter two scenarious, 1. Spacing is kept at its minimum value and 2. Spacing is kept the same line width, for various International Technology Roadmap for Semiconductor (ITRS) Technology nodel.

The total capacitance of the wire Equation (1):

$$C_t = C_g + 2C_c \quad (1)$$

Where:
C_g = The gate capacitance
C_c = The coupling capacitance Equation (2 and 3):

$$C_g = e\left(\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77} \times \left(\frac{t}{t+4.53h}\right)^{0.07}\right) \quad (2)$$

$$C_C = e\left(\begin{array}{l} 1.41\frac{t}{s}e^{\frac{-4s}{s+8.01h}} + 2.37\left(\frac{w}{w+0.31s}\right)^{0.28} \\ \times\left(\frac{h}{h+8.96s}\right)^{0.76} \times e^{\frac{-2s}{s+6h}} \end{array}\right) \quad (3)$$

Where:
t = The interconnect thickness
w = The interconnect width
h = The dielectric height
s = The spacing between the neighbor interconnects

The proposed Pre detective Technology Model (PTM) model library functions (http://public.itrs.net/Files/2001ITRS/Home) can be incorporated using nanometer technological specifications to optimize the power. The closed form expression for power dissipation is carried out in this study with buffer as well as without buffer Equation (4):

$$P_t = p_w - p_b \quad (4)$$

Where:
P_t = The total power dissipation
P_w = A without buffer power dissipation
P_b = A with buffer power dissipation

Global interconnects are comprised of wires and buffers. An optimal repeater insertion technique is used to minimize the wire length (shortest path between source to sinks), power dissipation and wire size. This wire size is inversely proportional to the power dissipation and buffer insertion is directly proportional to the power dissipation.

2.2. Single Long Uniform Wire Routing Without Buffer Insertion Approach

A single long 45 nm technological node wire interconnects is considered for routing. The gate capacitance C_g is kept as 1.92 fF/mm for each segment. The route length is calculated from source to sink represented by segments. The total capacitance is measured with respect to ground for x segments is calculated by 1.92fF×x. The total power is calculated without buffer insertion is Equation (5):

$$P_t = V_{dd} \times f_c \times C_{tg} \quad (5)$$

Where:
V_{dd} = A supply voltage in interconnect driven routing
f_c = A clock frequency
C_{tg} = The total gate capacitance

2.3. Single Long Uniform Wire Routing With Buffer Insertion Approach

The buffer is inserted to the Manhattan's bending degrades the power dissipation in the wire interconnect

signal. The total buffer insertion is limited to three. The power is dissipated by using wire segments and buffers from source to a sink node Swaminathan *et al*. (2013), the total power dissipation with buffer insertion is subtracted with the total power dissipation without buffer insertion is calculated and is given by Equation (6):

$$P_t = P_{tnb} - P_{twb} \quad (6)$$

Where:
P_{tnb} = The total power without buffer insertion
P_{twb} = the total power with buffer insertion

Kaur and Sulochanna (2013) the uniform buffer insertion is an efficient technique for driving long interconnects. The objective of a uniform buffer insertion is to minimize the power dissipation and delay a long interconnect.

The total power dissipation with buffer insertion is calculated by Equation (7):

$$P_{twb} = V_{dd} \times f_c \times (C_{gt} - n_b) + n_b \times b_{os} \quad (7)$$

Where:
n_b = The number of buffers
b_{os} = The buffer value in one segment

The total power dissipation without buffer insertion is represented by Equation (8):

$$P_{tnb} = V_{dd} \times f_c \times C_{gt} \quad (8)$$

The buffer is inserted in an interconnect signal wire connected from a source to a sink node. Hence the power dissipation gets degraded and is calculated.

2.4. Two Uniform Wire Routing Without Buffer Insertion Approach

The node wire dimension is assigned as 45 nm. Let S_{min} = W_{min} =102.5 nm. The parameters are taken from the Predictive Technology Model (PTM). The gate capacitances are 7.265 fF/mm and 1.92 fF/mm. V_{dd} = 1V, f_c = 15GH_Z. The total cross coupling capacitance is calculated by Equation (9):

$$C_{ct} = (C_{C1} + C_{C2} + C_{C3}) \times C_{cos} \quad (9)$$

where, C_{c1}, C_{c2}, C_{c3} are the coupling capacitances between two uniform parallel wire in three manhattan bending. C_{cos} is the coupling capacitance in one segment. The total gate capacitance is Equation (10):

$$C_{gt} = (C_{g1} + C_{g2} + C_{g3} + C_{g4} + C_{g5} + C_{g6}) \times C_{gos} \quad (10)$$

where, C_{g1}, C_{g2}, C_{g3} are the gate capacitance in wire one and C_{g4}, C_{g5}, C_{g6} are the gate capacitance value in wire two. The total capacitance is calculated by adding the total coupling capacitance and total gate capacitance. It is calculated by Equation (11):

$$C_t = C_{ct} + C_{gt} \quad (11)$$

The total Power dissipation in two uniform wire is calculated by Equation (12):

$$P_{tw} = V_{dd} \times f_c \times (C_{gt} + 2 \times C_{ct}) \quad (12)$$

The total power dissipation with buffer in Two uniform wire calculated by Equation (13):

$$P_{tb} = V_{dd} \times f_c \times (C_{gt} - n_b) + 2C_{ct} \times (n_b \times b_{os}) \quad (13)$$

The total power dissipation in the interconnect signal wires is calculated by Equation (14):

$$P_t = P_{tw} - P_{tb} \quad (14)$$

Now, the percentage of power saving due to the buffer insertion is calculated by Equation (15):

$$p_s = \frac{p_{tb}}{P_{tw}} \times 100 \quad (15)$$

Where:
P_{tw} = The total power dissipation without buffer
P_{tb} = The total power dissipation with buffer

2.5. Delay and Bandwidth Interconnections

The delay of the line segment is optimal. There fore the optimal delay per unit length can be obtained, (Yan *et al*., 2013; Narasimhan and Sridhar, 2010) Equation (16):

$$D = 2\sqrt{r_c c_0}\left(\frac{1}{2}\left(1 + C_b / C_0\right)\right)\frac{1}{\sqrt{rc}} \quad (16)$$

The global interconnection total delay D and the number of interconnects N decide the interconnect

bandwidth B with the optimal buffer insertion can be definded as (Yan *et al*., 2013) Equation (17 and 18):

$$B = \frac{N}{D} \tag{17}$$

$$B.W = \frac{1}{\ln 2 \times 2\sqrt{r_s c_0}}\left(1+\sqrt{\frac{1}{2}\left(1+\frac{C_b}{C_0}\right)}\right) \times \frac{1}{\sqrt{rc}}(w+s) \tag{18}$$

Where:
C_o = The input capacitance
C_p = The out put capacitance
r_s = The resistance

2.6. Interconnect Driven Routing Using PSO Algorithm

- Initialize each particle with a random velocity and random position
- Calculate the cost for each particle
- If the current cost is lower than the best value, treat the particle is gBest
- Calculate the new velocity and position to each particle
- Repeat steps 2-4 until maximum iteration or minimum error criteria is not attained

The algorithm is initialized with particles at random positions and then it explores the search space to find better solutions. In every itration, each particle adjusts its velocity to follow two best solutions (Datta *et al*., 2013) the first is the cognitive part, where the particle follows its own best solution found so far. This is the solution that produces the lowest cost (has the highest fitness). This value is called pbest (particle best) (Yusof *et al*., 2011; Tang and Mao, 2006). The other best value is the current best solution of the swarm, i.e., the best solution by any particle in the swarm. This value is called gbest (global best) (Kennady and Eberhart, 1995; Eberhart and Shi, 2001).

Each particle adjusts its velocity and position is given by Equation (19 and 20):

$$V_1 = V + C_1 \times R_1 \times (P_{best} - x) + C_2 \times R_2 \times (q_{best} - x) \tag{19}$$

$$X_1 = x + v_1 \tag{20}$$

Where:
V = The current velocity
V_1 = the new velocity
x = The current position
X_1 = The new position

R_1 and R_1 are distributed random numbers, C_1 and C_2 are acceleration coefficients. C_1 influences the cognitive behavior. i.e., how much the particle will follow its own best solution and C_2 is the factor for social behavior. i.e., how much the particle will follow the swarm's best solution. It has a limited number of parameters and the impact of parameters to the solutions is small compared to other optimization techniques. PSO algorithm determines the sortest path between source to sink. PSO algorithm determine the optimum power that dissipates within the constraint of three manhattan style routing bending with buffer insertion as agreed.

3. RESULTS

In this section, the power dissipation for various buffers is simulated through MATLAB simulations. The power dissipation is compared with various nanometer technology parameters.

Figure 2 and 3 show the power dissipation for number of buffers is simulated in various nanometer technological parameter values for single and two uniform wire routing. **Figure 1** shows the power saving for number of buffers is simulated in various nano meter technological parameter value for two uniform wire routing.

4. DISCUSSION

Figure 2 and 3 is shown that the number of buffers are increased, the power dissipation is also be incresed. It is clearly shown that at 65 nm power dissipation ismore when compared to 32 nm power dissipation. It is seen that for ten buffer insertion, for 32 nm technology model, the power dissipation value is 2×10^{11}, but for 65 nm technology model, the power dissipation value is 18×10^{11}. It is inferred that the power dissipation is same for both single and two uniform wire routing.

The **Table 1 and 2** w_{opt}, w_{opt}, s_{opt}, h_{opt}, k_{opt}, τ_{opt}, p_{opt} and B_{opt} are the optimal results with considering the self heating effect and w^1_{opt}, s^1_{opt}, h^1_{opt}, k^1_{opt}, τ^1_{opt}, p^1_{opt} and B^1_{opt} are the traditional optimization without considering the self heating effect which is from (Tang and Mao, 2006).

Figure 1 shows routing. It is shown that the number of buffers are increased, the power saving is also be increased. The power saving is maximum for 32 nm technology model when compared with 45 nm technology model. It is seen that 32 and 65 nm technology models power saving is the same.

Table 1. Comparision of interconnect dimension parameters between two kinds of optimization results

	Tech node (nm)	w^{opt} (mm)	w^{1}_{opt}(mm)	s^{opt} (mm)	s^{1}_{opt}(mm)	h^{opt} (mm)	h^{1}_{opt} (mm)	k^{opt}	k^{1}_{opt}
Previous	90	972	898	398	353	2.1	1.4	86	81
Work (Yan *et al*.,	65	886	774	336	298	1.7	0.9	77	69
2013)	40	657	536	232	214	1.1	0.5	59	51
Proposed Work	32	556	422	104	110	1.8	0.2	32	26

Table 2. Comparision of interconnect delay, power dissipation and band width between two kinds of optimization results

	Tech node	τ_{opt}	τ^{1}_{opt}	p^{opt}	p^{1}_{opt}	B^{opt}	B^{1}_{opt}
Previous	90	101.3	120.3	0.21	0.26	2.63	2.36
Work (Yan *et al*., 2013)	65	76.2	89.40	0.58	0.64	2.84	2.43
	40	94.4	110.5	1.39	1.50	3.17	2.75
Proposed Work	32	82.6	95.30	2.18	2.52	3.59	2.83

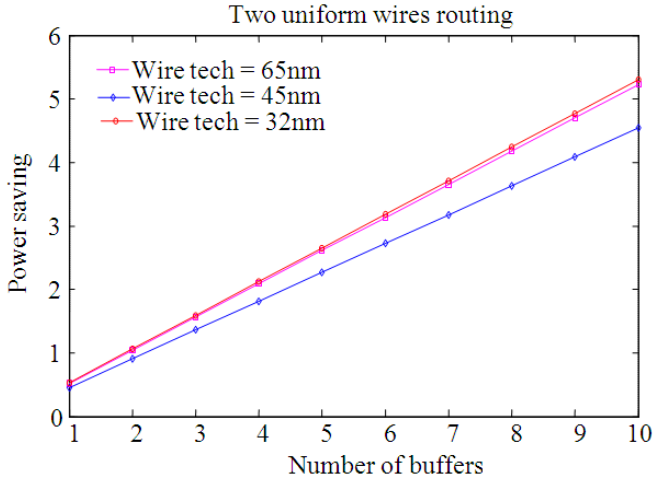

Fig. 1. Total power saving Vs number of buffer in two uniform wire routing

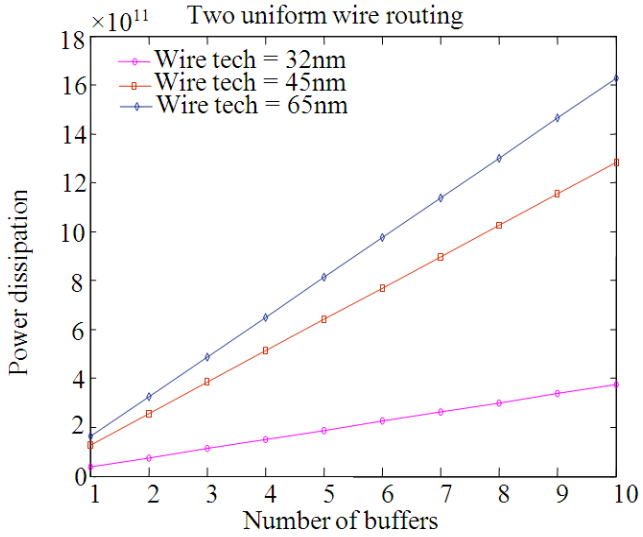

Fig. 2. Total power dissipation Vs number of Buffers in single uniform wire routing

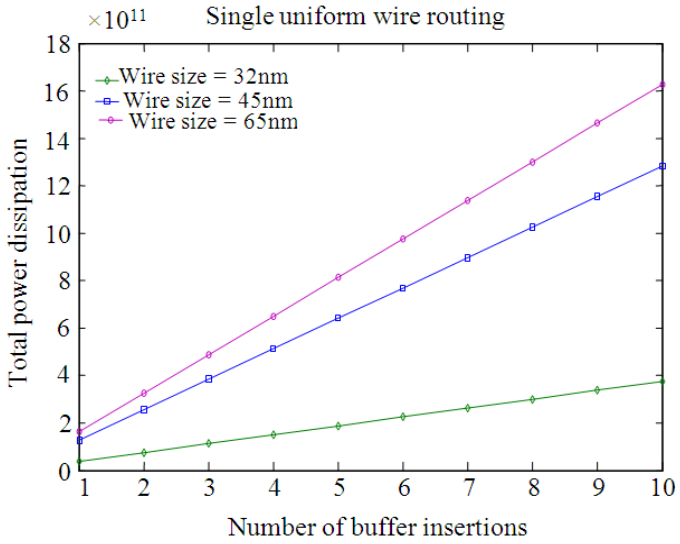

Fig. 3. Total power dissipation Vs number of Buffer in two uniform wire routing

The global interconnection power distribution is inversely professional to the width and spacing of the interconnection. which is same as that of the delay. Solower power distribution requires large nterconnection width and spacing. The aim of the global interconnect design is to get a small delay per unit length, low power dissipation and large bandwidth simultaneously unfortunately, it can be seen from the above discussion, small delay and low power dissipation, require large interconnection width and spacing. But large bandwidth requires small interconnection width and spacing (Tep and Yusof, 2010).

Table 2 The interconnection less delay, less power dissipation and large bandwidth can be achieved compared to my work. **Table 1** shows the optimal wire width w_{opt}, s_{opt} buffer size k_{opt} and the length h_{opt} between two buffers considering the self heating effect is larger than without considering the self heating.

5. CONCLUSION

The optimal power dissipation for simultaneous buffer insertion and buffer sizing and wire sizing with shortest path constraints using PSO algorithm for VLSI interconnect driven routing has been investigated and analyzed. The closed form expressions for minimizing the total power dissipation using shortest path is calculated. The closed form solutions can be used to efficiently estimate the power dissipation in the stages of the VLSI designs. The simulation results show that the simultaneous buffer insertion/sizing and wiring sizing is better than traditional uniformed buffer insertion in terms of optimal shortest path and optimal power allocation. The self heating effect, the interconnection wire delay, power dissipation and bandwidth, which depend on the interconnect resistance per unit length and capacitance, are analyzed. The proposed optimal model is validated and compared on 90, 65, 40 and 32 nm cmos technology. Performance analysis in this study will facilitate future work on new technology specifications and improved power dissipations and bandwidth and decrese the delay.

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