Performance Analysis of Different Optical Switching Architectures

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Abstract: Problem statement: Optical Packet Switching (OPS) and transmission networks based on Wavelength Division Multiplexing (WDM) have been increasingly deployed in the Internet infrastructure over the last decade in order to meet the huge increasing demand for bandwidth. Several different technologies have been developed for optical packet switching such as space switches, broadcast-and-select, input buffered switches and output buffered switches. These architectures vary based on several parameters such as the way of optical buffering, the placement of optical buffers, the way of solving the external blocking inherited from switching technologies in general and the components used to implement WDM. **Approach:** This study surveys most of the exiting optical packet switching architectures. A simulation-based comparison of input buffered and output buffered architectures were presented. **Results:** The performance analysis of the selected two architectures derived using simulation program and compared at different scenarios. We found that the output buffered architectures give better performance than input buffered architectures. **Conclusion:** The simulation results shows that the-broadcast-and-select architecture is attractive in terms that it has lees number of components compared to other switches.

Key words: Input-Output Switch, Optical packet switching (OPS), Packet loss probabilities, Performance analysis, Wavelength Division Multiplexing (WDM), Random Access Memory (RAM), optical gate, buffer

INTRODUCTION

Optical Packet Switching (OPS) and transmission networks based on Wavelength Division Multiplexing (WDM) have been increasingly deployed in the Internet infrastructure over the last decade in order to meet the huge increasing demand for bandwidth (Masetti *et al*., 1996; Danielsen *et al*., 1997; Chang and Mehta, 2010). An optical packet network consists of optical packet switches interconnected with fibers running WDM. The switches may be adjacent or connected by light paths. A light path is a circuit-switched connection consisting of the same wavelength allocated on each link along the path. It may consist of different wavelengths along the path if converters are present. The user data is transmitted in optical packets, which are switched within each optical packet switch entirely in the optical domain. Thus, the user data remains as an optical signal in the entire path from source to destination. No optical-to-electrical or electrical-to-optical conversions are required.

Packet switches based on photonics have some potential advantages over their electronic counterparts.

Some studies have shown that the ultimate capacity of photonics-based switches will exceed the capacity of large electronic switching nodes (Masetti *et al*., 1996; Zhang, T *et al*., 2006). Another advantage offered by photonics is the potential of optical transparency. Transparency means that, except for the packet header, the packet payload can be encoded in an arbitrary format and at an arbitrary bit rate. In addition, Wavelength Division Multiplexing (WDM) can be exploited to increase the switching performance since more than one packet can be carried by different wavelengths at the same time and the same input/output port.

One difficulty in the implementation of optical packet switching systems is the lack of optical Random Access Memory (RAM). There has been much effort to investigate and develop optical RAM's (Kasahara *et al*., 1988). Unfortunately, optical RAM suitable for optical packet switching has not yet been found (Kasahara *et al*., 1988; Suzuki and Kasahara, 1992). The alternative is to use optical fiber delay-lines incorporating other optical components such as optical gate switches, optical couplers and amplifiers to realize optical packet buffering (Tucker, 2008; Hass, 1993; Spring and Tucker, 1993; Sasayama *et al*., 1993; Zhong *et al*., 1994).

Several different technologies have been developed for optical packet switching such as space switches, broadcast-and-select, input buffered switches and output buffered switches. These architectures vary based on several parameters such as the way of optical buffering, the placement of optical buffers, the way of solving the external blocking inherited from switching technologies in general and the components used to implement the WDM.

In this study, we survey most of the existing architectures and compare their performance. Our simulation-based comparisons analyze and compares the performance of two selected architectures.

MATERIALS AND METHODS

When two packets from different input ports must be switched to the same output port at the same time, contention arises. This is a problem that commonly arises in packet switches and is known as external blocking. In this case, the switch controller and the switch fabric must employ some strategy to resolve the contention. Output port contention can be resolved in three domains: in wave-length domain (using converters), in time domain (using fiber delay lines), or in space domain (using deflection routing). Strategies that combine more than one method are also possible. Most of the OPS architectures use fiber delay lines and/or wavelength converter to solve the contention problem. Below we discuss these two solutions.

Contention resolution in time domain: Optical buffering. The lack of an efficient way to store information in the optical domain represents a major difficulty in the design of OPS nodes. Research has focused on ways of emulating electronic RAM capabilities through the use of Fiber Delay Lines (FDLs) to delay optical signals (Hunter *et al.*, 1998a; Hunter *et al.*, 1998b; Ramamurthy and Mukherjee, 1998). An FDL can delay a packet for a specified amount of time, which is related to the length of the delay line and the speed of light. A buffer for D packets with a FIFO discipline can be implemented using D fiber delay lines whose lengths are equivalent to multiple of slots. A slot, T, is the time required for a packet to be transmitted and propagated from an input port to an output port. As shown in Fig. 1, delay line *i* delays a packet for *i* time slots. A counter keeps track of the number of packets in the buffer. It is decreased by 1 when a packet leaves the buffer and increased by 1 when a packet enters the buffer. Suppose that the value of the counter is j when a packet arrives at the buffer; then the packet will be routed to the jth delay line.
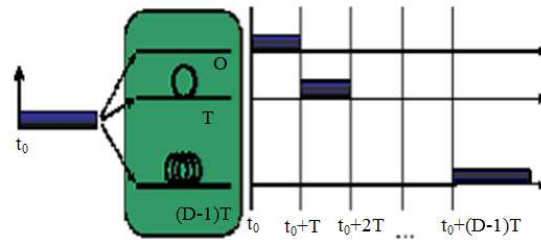

Fig. 1: An optical buffer based on fiber delay lines

However, the delay is chosen at packet arrival and a packet is lost when the required delay is larger than the maximum delay available which is (D -1)T.

It is worth to mention that FDL-based buffers are able to store multiple packets with the constraint that only one packet enters and leaves the buffer at a time, unless WDM is invoked. Also, similar to their electronic counterpart, optical buffers may be placed at the input, output, or both, of a packet switch. However, limited by the length of the delay lines, this type of buffer is usually small and does not scale up.

Contention resolution in wavelength domain: In WDM, several wavelengths run on a fiber link that connects two optical switches. This can be exploited to minimize external blocking by means of wavelength conversion. Wavelength conversion (Ramamurthy and Mukherjee, 1998; Elmirghani and Mouftah, 2000; Rekha and Ramalingam, 2009) is the ability to convert an optical signal on a given input wavelength to some other output wavelength. This can be used as a mechanism for contention resolution that can improve the utilization of resources in an OPS. Let us assume that two packets are destined to go out of the same output port at the same time. Then they can be still transmitted out, but on two different wavelengths. This method may have some potential in minimizing external blocking, particularly since the number of wavelengths that can be coupled together onto a single fiber continues to increase. More detailed discussion and comparison of wavelength converter technologies can be found in (Elmirghani and Mouftah, 2000). As a contention resolution method, wavelength conversion has some highly desirable properties in that it does not introduce delays in the data path and it does not cause packet resequencing.

Converters may be fixed or tunable and can be placed at the input and/or output ports of an optical packet switch; moreover, each port of the switch may be equipped with its own dedicated converter, or the

converters may be shared by all ports. Consequently, a variety of switch architectures are possible depending on the availability and placement of converters.

Optical switch architectures: A wide variety of switch fabric architectures have been proposed for OPS. In general, we can classify the switch architectures to the following classes:

- Space switch architectures
- Broadcast and select switch architecture
- Input buffered switch architecture
- Output buffered switch architecture

In the following subsections, we discuss each of these architectures.

Space switch architecture: Space switch fabric architecture is shown in Fig. 2 (Glance *et al.*, 1993). The switch consists of N incoming and N outgoing fiber links, with W wavelengths running on each fiber link. The switch is slotted and the length of the slot is such that an optical packet can be transmitted and propagated from an input port to an output port.

The switch fabric consists of three parts: Optical packet encoder, space switch and optical packet buffer. The optical packet encoder works as follows. For each incoming fiber link, there is an optical de multiplexer which divides the incoming optical signal to the W different wavelengths. Each wavelength is fed to a different Tunable Wavelength Converter (TWC) which converts the wavelength of the optical packet to a wavelength that is free at the destination optical output buffer. Then, through the space switch fabric, the optical packet can be switched to any of the N output optical buffers. Specifically, the output of a TWC is fed to a splitter which distributes the same signal to N different output fibers, one per output buffer. The signal on each of these output fibers goes through another splitter which distributes it to D + 1 different output fibers and each output fiber is connected through an optical gate to one of the FDLs of the destination output buffer. The optical packet is forwarded to an FDL by appropriately keeping one optical gate open and closing the rest. The information regarding to which wavelength a TWC should convert the wavelength of an incoming packet and the decision as to which FDL of the destination output buffer the packet will be switched to is provided by the control unit, which has knowledge of the state of the entire switch.

Each output buffer is an optical buffer implemented as follows. It consists of D + 1 FDLs, numbered from 0 to D. FDL i delays an optical packet for a fixed delay equal to i slots. FDL 0 provides zero delay and a packet arriving at this FDL is simply transmitted out of the output port. Each FDL can delay optical packets on each of the W wavelengths. For instance, at the beginning of a slot, FDL 1 can accept up to W optical packets, 1/wavelength and delay them for 1 slot. FDL 2 can accept up to W optical packets at the beginning of each time slot and delay them for 2 slots. That is, at slot t, it can accept up to W packets (1/wavelength) and delay them for 2 slots, in which case these packets will exit at the beginning of slot t + 2. However, at the beginning of slot t1 it can also accept another batch of W optical packets. Thus, a maximum of 2W packets may be in transit within FDL 2; similarly for FDL 3 through D. The performance of optical space switch is analyzed in (Elmirghani and Mouftah, 2000).

Broadcast-and-select switch architecture. Figure 3 shows the architecture of a broadcast-and-select switch proposed as part of the European ACTS KEOPS project (Guillemot *et al.*, 1998). The switch has N input and output ports and it is equipped with D FDLs such that a packet can be delayed for an integer multiple of the slot time T, up to DT. The architecture in Fig. 3 assumes that each input fiber carries only one wavelength that is different than the wavelengths carried by the other input fibers; hence the total number of wavelengths is N. The switching fabric consists of three blocks: encoder, buffer and selector. The wavelength encoder block consists of N Fixed Wavelength Converters (FWCs), one per input and a multiplexer. The buffer block consists of a splitter, D FDLs and a space-switching stage implemented by means of splitters, optical gates and combiners. Finally, the wavelength selector block consists of N wavelength channel selectors implemented by means of de multiplexers, optical gates and multiplexers. These three blocks make up the broadcast-and-select switch fabric.

The switch is slotted. At the beginning of a time slot, each wavelength converter in the wavelength encoder block converts the wavelength of the incoming packet to a fixed wavelength. The output of the N converters is combined and then distributed through a splitter into D different FDLs. Each FDL has a different delay which is an integer number of slots. That is, FDL i has a delay of i slots. The N optical packets are stored simultaneously to the D different FDLs. At the beginning of the next slot, a maximum of D * N optical packets exit from the D FDLs and up to N of them are directed to their destination output ports without any collisions.
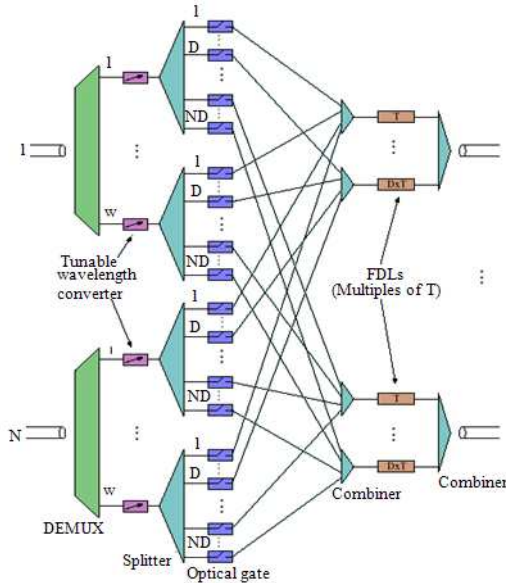
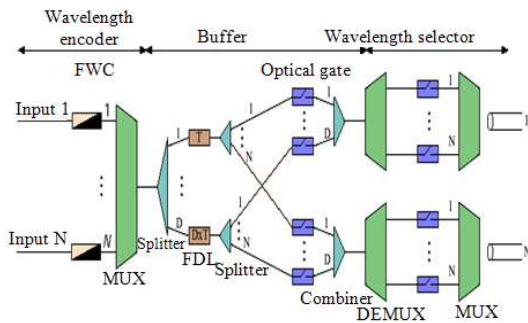Fig. 2: Space switch architecture with N ports, W wavelengths and D FDLs

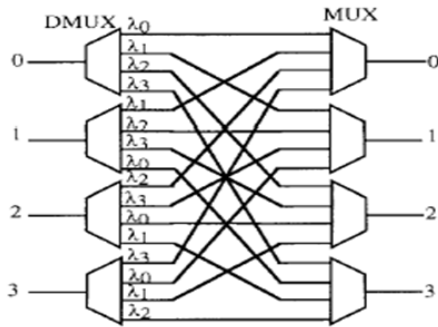Fig. 3: Broadcast-and-select switch architecture with N ports, W wavelengths and *D* FDLs

Fig. 4: 4*4 Arrayed-Waveguide Grating (AWG) multiplexers

This is achieved through a combination of splitters, optical gates, de multiplexers and multiplexers. Specifically, the output signal from each FDL goes through a splitter which distributes it over N outputs. We recall that this output signal consists of N multiplexed optical packets, one for each wavelength. The signal from output *j* of each splitter is directed to output port *j*. Since there are D such splitters, there are D such output signals, of which only one is selected and directed to output port *j*. This selected output signal is fed into a de multiplexer, which breaks it up into the N wavelengths, of which only one is transmitted out. The operation of this broadcast-and-select switch fabric is managed by a control unit. Note that performing broadcast or multicast transmission is straight-forward: all that is needed is for multiple output ports to select the same packet.

Optical packet buffer based on wavelength routing: A new wavelength routing-based packet buffer is presented in (Zhong and Tucker, 1998). It is based on Arrayed-Waveguide Grating (AWG) multiplexers (Takahashi *et al*., 1990; Dragone, 1991; Ab-Rahman *et al*., 2009) and wavelength conversion techniques (Durhuus *et al*., 1996; Glance *et al*., 1993). In order to explain the operation of this kind of buffer, we should first explain the wavelength routing model of an AWG. Consider a K * K AWG and let be the wavelengths operating in each port of the AWG (Takahashi *et al*., 1990). The wavelength that connect the *i*-th input to the *j*-th output of the AWGM can be expressed by $\lambda(i, j) = \lambda_q$ where:

$$q = (i + j) \bmod K \tag{1}$$

In other words, packet entering from port *i* and destining to port j will be converted to wavelength according to equation (1). For example, consider the 4 * 4 AWG shown in Fig. 4. Suppose that there is a packet in input port number 0 that needs to be switched to output port number 3. The wavelength of this packet will be converted to (q = (0+3) mod 4 = 3) which connects input port 0 to output port 3.

As mentioned above, a new wavelength routing-based optical packet buffer is presented in (Zhong and Tucker, 1998) and it is based on Arrayed-Waveguide Grating (AWG) multiplexers. As shown in Fig. 5, this optical packet buffer consists of a pair of AWGs (Takahashi *et al*., 1990; Dragone, 1991) and a set of D optical fiber delay lines connecting AWGs. The buffer has L input ports and L output ports, through which L packet streams can simultaneously access to the buffer.
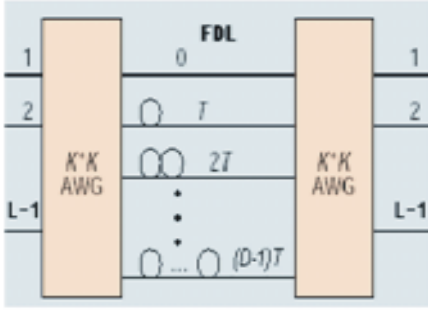
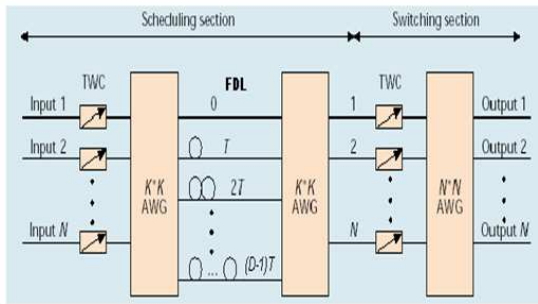Fig. 5: Wavelength routing based optical packet buffer

Fig. 6: Input buffered optical packet switch

The delay lines are numbered 0,1 ,2 ,…, (D - 1) from top to bottom. The i-th delay line has a delay amount of packet duration (slot), T. Note that the buffer has L input/output ports and D FDLs. Therefore, we need an AWG with K input/output ports where K = max (L,D).

Consider the case where L = D = K. With reference to Fig. 5 and the relationship of wavelengths connecting the inputs and outputs of a AWG, it can be seen that WDM packets entering the buffer at the i-th input port will be routed (or de multiplexed) to different outputs of the first AWG, according to their wavelengths. After passing through different lengths of delay lines, these packets are multiplexed by the second AWG and then leave the buffer from the i-th output port. In other words, a packet entering the buffer at the i-th input port will leave the buffer from the i-th (same input port index) output port after receiving a certain delay time determined by the packet wavelength. Note that a packet with a given wavelength entering the buffer at a different input port will receive a different packet delay. For example, a packet of wavelength λ_2 entering at the zeroth input port will receive a delay with a two slots (2T); while a packet of the same wavelength, λ_2, entering at the 1st input port will receive a delay with

one slot (T). Therefore, the delay received by a packet is determined by the wavelength of the packet and by the input port at which the packet enters the buffer. On the other hand, if a packet entering the buffer at the i-th input port requires a delay of a Q slots (i.e., QT), the packet has to be converted to wavelength λ_q (Durhuus *et al.*, 1996; Glance *et al.*, 1993) where q is given by:

$$q = (Q + i) \bmod K \tag{2}$$

Input-buffered switch architecture: This switch was proposed in (Danielsen *et al.*, 1997) and is shown in Fig. 6. Each incoming and outgoing link carries a single wavelength. The wavelength of an output port varies with packets. The switch consists of the scheduling part and the switching part.

The scheduling part is used for contention resolution and is composed of N TWCs, one for each incoming wavelength, two K x K Arrayed Waveguide Gratings (AWGs) and D FDLs, where K = max(N, D). Buffering in the scheduling part is based on the optical wavelength routing-based buffering discussed in the previous part. i.e., a packet entering input i of the first AWG will appear at output i of the second AWG after a specified delay. The delay of an optical packet is selected using the following two rules: first, no two optical packets may appear at the same slot at the same switch output; second, no two optical packets may appear at the same buffer output at the same slot.

The switching part is used for switching optical packets to their destination output ports and is made up of an AWG and TWCs. The TWCs are used to assign the optical packet the right wavelength corresponding to the desired output port. This kind of architecture suffers from head-of-line blocking, which is inherent in input buffering switches. For example, suppose that optical packet 1 in input i must be routed to output 1, while optical packet 2 behind optical packet 1 in input i must be routed to output 2. If optical packet 1 must be delayed for one time slot, optical packet 2 has to be delayed for at least one time slot due to the second rule, even though optical packet 2 goes to a different output port.

Output-buffered switch architecture: Fig. 7 shows the schematic of an N * N output-buffered optical packet switch. It consists of a set of N TWC, an N * N optical space switch matrix and an N * N wavelength routing-based packet buffer. The N * N optical space switch performs the switching of packets to their desired outputs.
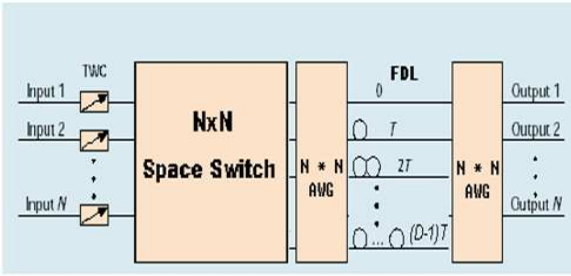
Fig. 7: Output buffered switch architecture

Unlike the input-buffered packet switch, the N * N optical space switch in Fig. 7 cannot be replaced by a set of N TWC's and an N * N AWG. This is because, if the N * N optical space switch is replaced by a set of N TWC's and an N * N AWG, then up to N packets may appear at a given output of the AWG.

In this architecture, there may be more than one packet destined for the same output in a time slot, resulting in packet contention. However, this packet contention is resolved by wavelength conversion and wavelength routing-based buffering. More specifically, in each time slot, packets that are destined for the same output will be shifted to different wavelengths before they are routed to the desired output by the optical space switch. Since these packets have been given different wavelengths by the wavelength converters at the input of the switch, they will receive different packet delays at the succeeding wavelength routing-based buffer so that only one packet will emerge at a given output of the switch in any time slot and hence packet contention is resolved.

RESULTS

So far we discussed several optical packet switching architectures. Performance analysis of the space switch and broadcast-and-select architectures is available in (Elmirghani and Mouftah, 2000; Zhong and Tucker, 1998) respectively. In this study, two simulation programs for input buffered and output buffered architectures have been developed. The average packet delay and packet loss probability for these two architectures are compared under different number of Fiber Delay Lines (FDLs).

Both simulations assume a random traffic model in (Hluchyj and Karol, 1988): (1) each input has an identical and independent arrival of packets with a probability p in any time slot and (2) each packet is equally likely destined for any of the outputs. The probability *p* can also be seen as the offered traffic load at each input. Upon packet arrival, a scheduling algorithm is invoked in order to assign an ideal time

slot to the arriving packet according to its destination. If no available slot, the packet will be lost. The main purpose of packet scheduling algorithm is to prevent packet contention. More specifically, concurrent packets arriving at different inputs and destined for the same output will be given different delays in the scheduling part. The delay of a packet in the scheduling part is in turn determined by the wavelength to which the packet is converted. The function of packet scheduling is to allocate a minimum time delay to each packet, subject to the following two conditions in any time slot: (1) no two packets will be addressed to the same output of the switching part and (2) no two packets will appear at a given input of the switching part. A packet that cannot be assigned a time slot is blocked by turning off the corresponding TWC at the scheduling part and hence lost.

Figure 8(a)-(c) show the relation between packet loss probability and offered traffic load *p* of input buffered optical packet switch for various buffer capacities D (number of fiber delay lines), when the switch size N is 16, 32 and 64, respectively.

As expected, the packet loss probability is substantially reduced by increasing the buffer capacity, which effectively increases the number of available time slots.

Similarly, Fig. 9(a)-(c) show the relation between packet loss probability and offered traffic load *p* of input buffered optical packet switch for various buffer capacities D (number of fiber delay lines), when the switch size N is 16, 32 and 64, respectively. It shows also the packet loss probability is substantially reduced by increasing the buffer capacity, which effectively increases the number of available time slots.

When comparing the packet loss probability of the input buffered delay and the output buffered delay architectures vs. the offered load for different switch sizes as shown in Fig. 10, we found the following:

- The output buffered architecture has less packet loss probability for all buffer sizes. This is because that input buffered switches suffer from head-of-line blocking which results in more packet droppings
- For a given offered traffic load and a given buffer capacity (i.e. fixed D), the packet loss probability is almost independent of the switch size for both input buffered and output buffered switches. As shown in Fig. 10, each of the two architectures has almost the same packet loss probability curves for all packet sizes. Note that the legend "OB 16×16" used in this Fig. 10 means output buffered 16 * 16 switch. Similarly "IB 16×" means input buffered 16 * 16 switch
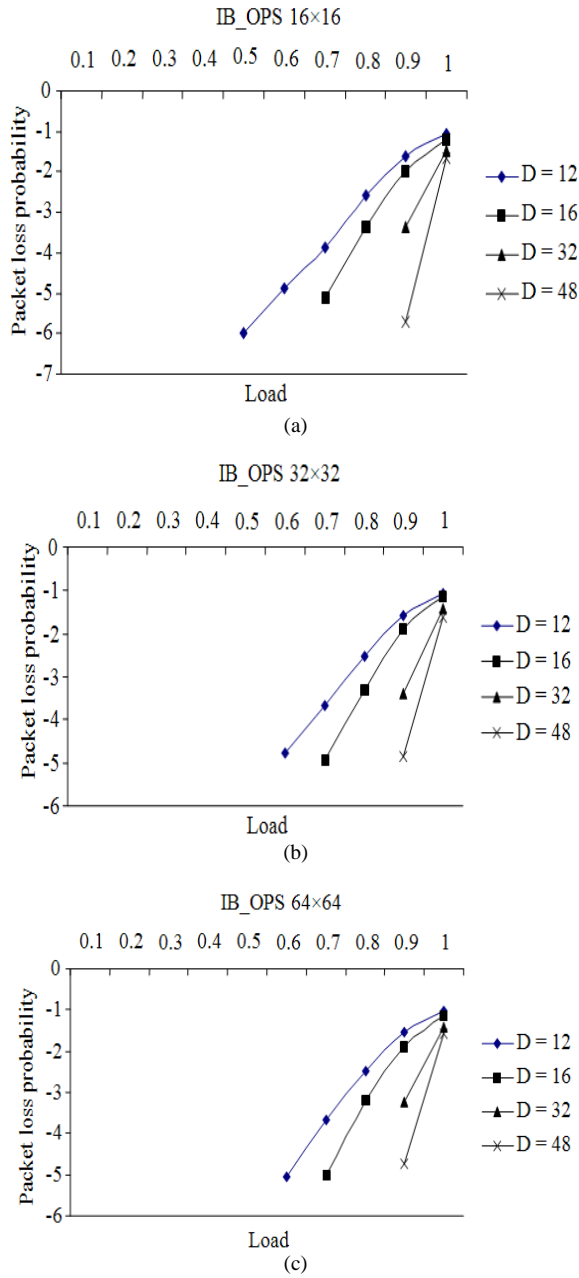
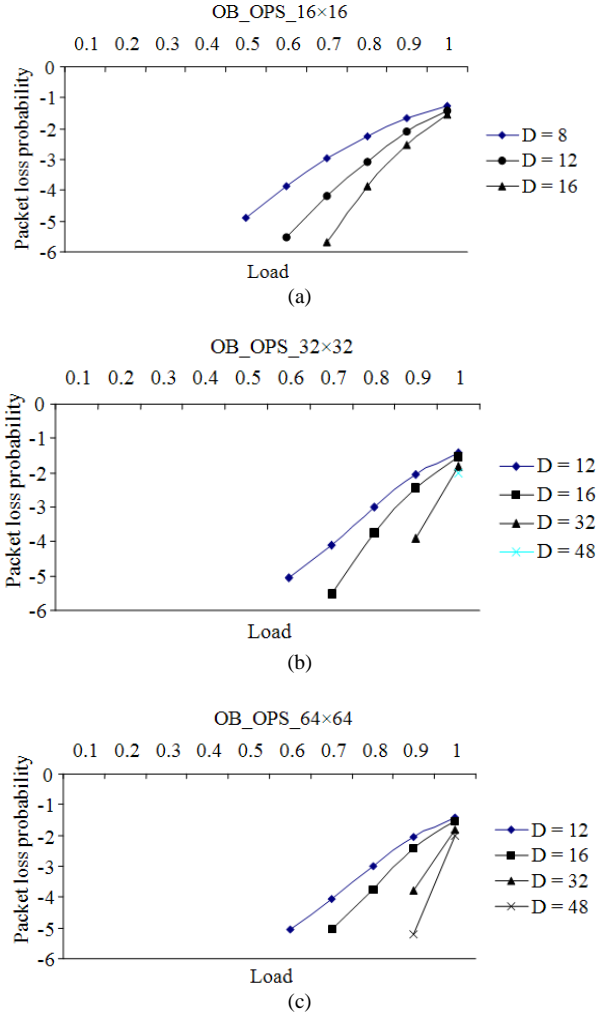Fig. 8: (a) 16 * 16 OPS. (b): 32 * 32 OPS. (c): 64 * 64 OPS
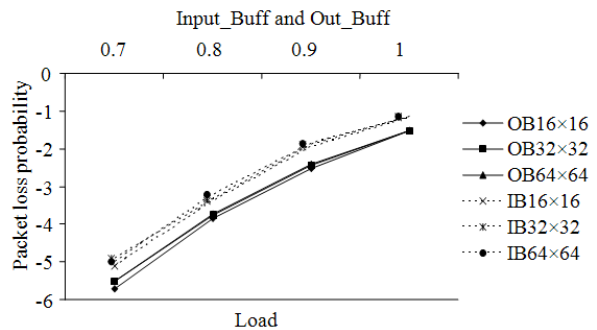

Fig. 9 (a): 16 * 16 OPS. (b): 32 * 32 OPS. (c): 64 * 64 OPS

Fig. 10: Comparing packet loss probabilities for input buffered and output buffered architectures for different switch sizes
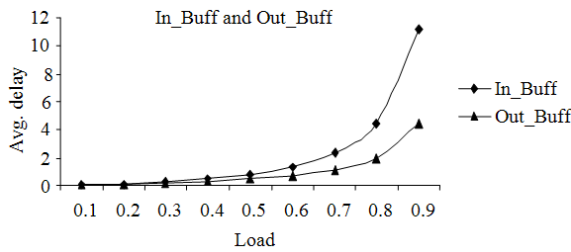
Figure 11 shows the packet delay (in terms of time slots) versus offered traffic load for a switch size of N = 64 and a number of delay lines of D = 64. It can be seen that the output-buffered switch has better delay performance. By fixing the switch size N to 64 and offered load p to 0.8, we show the relation between the packet loss probability and the number of fiber delay lines, FDLs in Fig. 12.

Fig. 11:Delay versus offered load for input buffered and output buffered architectures for switch size N = 64 and number of FDLs, D = 64

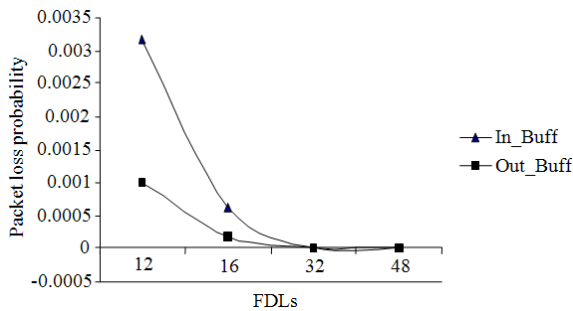Fig. 12: Optimal number of FDLs for N=64 and p = 0.8

This Fig. 12 shows that the optimal (minimum) number of FDLs for both input buffered and output buffered architectures that ensures a packet loss probability less than 10^{-6} is D = 32.

Finally, the switching speed of the input buffered and output buffered switched is computed through the simulation. In our measurement, we keep feeding packets to input ports until the packet loss probability becomes grater than 10^{-6}. We found that the input buffered switch can operate in 2.5 Gbps while the output buffered switch can operate in 10 Gbps.

CONCLUSION

In this study we have surveyed most of the exiting optical packet switching architectures. A simulation-based comparison of input buffered and output buffered architectures is presented. We found that the output buffered architectures give better performance than input buffered architectures. Another comparison based on the components involved in various architectures is also presented. The-broadcast-and-select architecture is attractive in terms that it has lees number of components compared to other switches.

REFERENCES

Ab-Rahman, M.S., B. Ng, N.M. Ibrahim and S. Shaari, 2009. Low-Cost Encoding Device for Optical Code Division Multiple Access System. Am. J. Eng. Applied Sci., 2: 317-323. DOI: 10.3844/ajeassp.2009.317.323

Chang, C. and R. Mehta, 2010. Fiber optic sensors for transportation infrastructural health monitoring. Am. J. Eng. Applied Sci., 3: 214-221. DOI: 10.3844/ajeassp.2010.214.221

Danielsen, S.L. *et al.*, 1997. WDM packet switch architectures and analysis of the influence of tunable wavelength converters on performance. J. Lightwave Technol., 15: 219-227. DOI: 10.1109/50.554327

Dragone, C., 1991. An N _ N optical multiplexer using a planar arrangement of two star couplers. IEEE Photon. Technol. Lett., 3: 896-899. DOI: 10.1109/68.84502

Durhuus, T. *et al.*, 1996. All-optical wavelength conversion by semiconductor optical amplifiers. J. Lightwave Technol., 14: 942-954. DOI: 10.1109/50.511594

Elmirghani, J.M.H. and H.T. Mouftah, 2000. All-optical wavelength conversion: Technologies and applications on DWDM networks. IEEE Communications Magazine, 38: 86-92. DOI: 10.1109/35.825645

Glance, B.S. *et al.*, 1993. New advances on optical components needed for FDM optical networks. J. Lightwave Technol., 11: 882-889. DOI: 10.1109/50.233252

Guillemot, C. *et al.* 1998. Transparent optical packet switching: The European ACTS KEOPS project approach. J. Lightwave Tech-nology, 16: 2117-2134. DOI: 10.1109/LEOS.1999.811768

Hass, Z., 1993. The staggering switch: An electronically controlled optical packet switch. J. Lightwave Technol., 11: 925-936. DOI: 10.1109/50.233257

Hluchyj, M.G. and M.J. Karol, 1988. Queueing in high-performance packet switching. IEEE J. Select. Areas Commun., 6: 1587-1597. DOI: 10.1109/49.12886

Hunter, D.K., M.C. Chia and I. Andonovic, 1998a. Buffering in optical packet switches. J. Lightwave Technol., 16: 2081-2094. DOI: 10.1109/50.736577

Hunter, D.K., W.D. Cornwell, T.H. Gilfedder, A. Frenzen and I. An-donovic, 1998b. SLOB: A switch with large optical buffers for packet switching. J. Lightwave Technol., 16: 1725-1736. DOI: 10.1109/50.721059

Kasahara, K. *et al*., 1988. Double heterostructure optoelectronic switch as a dynamic memory with low power consumption. Appl. Phys. Lett., 52: 679-681. DOI: 10.1063/1.99345

Masetti, F. *et al*., 1995. ATMOS (ATM optical switching): Results and conclusions of the RACE R2039 project. In Proceeding of the ECOC'95, pp: 645-652. http://hdl.handle.net/1854/LU-254082

Masetti, F., *et al.*, 1996. High speed, high capacity ATM optical switches for future telecommunications transport networks. IEEE J. Select. Areas Commun., 14: 979-998. DOI: 10.1109/49.510922

Ramamurthy, B. and B. Mukherjee, 1998. Wavelength conversion in WDM networking. IEEE J. Selected Areas Commun., 16: 1061-1073. DOI: 10.1109/49.725178

Rekha, R.K. and A. Ramalingam, 2009. Optical Nonlinear Proreties and Optical Limiting Effect of Metanil Yellow. Am. J. Eng. Applied Sci., 2: 285-291.DOI**:** 10.3844/ajeassp.2009.285.291

Sasayama, K., K. Habara, W.D. Zhong and K. Yukimatsu, 1993. Photonic ATM switch using frequency-routing-type time-division interconnection network. Electon. Lett., 29: 1778-1779. DOI: 10.1049/el:19931184

Spring, J. and R.S. Tucker, 1993. Photonic 2 _ 2 packet switch with input buffers. Electron. Lett., 29: 284-285. DOI: 10.1049/el:19930194

Suzuki, S. and K. Kasahara, 1992. Electro-photonic devices for gigabit networks. IEEE LTS, pp: 36-40. DOI: 10.1109/80.167002

Takahashi, H. *et al*., 1990. Arrayed-waveguide grating for wavelength division multi/demultiplexer with nanometer resolution. Electron. Lett., 26: 87-88. DOI: 10.1049/el:19900058

Tucker, R.S., 1995. Photonic packet switching. In Proceeding of the OFC'95 , Tutorial, Feb., pp: 4-28. DOI: 10.1109/OFC.2008.4528328

Tucker, R.S., 2008. Optical Packet-Switched WDM Networks: A Cost and Energy Perspective. Optical Fiber Communication Conference, San Diego California 24-28 Feb., pp. 1-25. DOI: 10.1109/OFC.2008.4528328

Zhong, W.D. and R.S. Tucker, 1998. Wavelength routing-based photonic packet buffers and their applications in photonic packet switching systems. Osa J. Lightwave Technol., 16. DOI: 10.1109/50.721060

Zhong, W.D., M. Tsukada, K. Yukimatsu and Y. Shimatsu, 1994. Terahipas: A modular and expandable terabit/second hierarchically multiplexing photonic ATM switch architecture. J. Lightwave Technol., 12: 1307-1315. DOI: 10.1109/50.301823

Zhang, T. *et al*., 2006. Shared fiber delay line buffers in asynchronous optical packet switches. IEEE J. Selected Areas Commun., 24:. 118-127. DOI: 10.1109/JSAC.2006.1613777