American Journal of Engineering and Applied Sciences

Technical Report

Design of an 8-bit Incremental ADC

[1,2]Zehong Cao, [1]Ze Chen and [1]Xinlong Cai

[1]Department of Electronic Engineering, Faculty of Engineering,
The Chinese University of Hong Kong, Hong Kong, China
[2]Faculty of Engineering & IT, University of Technology Sydney, Sydney, Australia

Article history
Received: 17-05-2018
Revised: 23-05-2018
Accepted: 31-05-2018

Corresponding Author:
Zehong Cao
Department of Electronic Engineering, Faculty of Engineering, The Chinese University of Hong Kong, Hong Kong, China
Email: zhcaonctu@gmail.com

Abstract: This technical report demonstrated a design an 8-bit switched-capacitor incremental ADC in UMC 0.13 μm CMOS. The design requirements are Supply voltage: 1.2V, Reference voltage (Vref): 1V, Resolution: 8 bits, Output data rate: 100 samples per second and Input voltage range: 0V to 1V. Furthermore, the determine the architecture of incremental A/D converter involved in fuzzy theory. The output waveforms of the clock generator plot with a proper time scale. In the result, we showed the digital outputs and plot the waveforms at the comparator's output for three DC input values: One near 0V, one near Vref/2 and one near Vref. The exact DC values give the offset and gain errors of proposed circuit, supported by simulation results. We also simulated the DNL and INL using a histogram method and give the plots of the DNL and INL of the ADC for all output. Finally, we conclude the case report with a discussion of results (comparison, problems, solution, possible improvements, etc.).

Keywords: Design, 8-bit, Incremental ADC, Voltage

Introduction

Architecture of the ADC

Because this very design only requires an output data rate of 100 samples per second, which is relatively low, first-order ADC should be sufficient to satisfy the requirement (A/DCHT, 2012). The conceptual diagram of this first-order ADC is shown below.

According to Fig. 1, the ideal ADC described as follows. Φ1 and Φ2 are non-overlapping opposite clocks and Φ1 will first be high. Since the output rate is 100 samples per second and this is an 8-bit ADC, the clock period of Φ1 and Φ2 is 1/(100×28) = 3.90625×10-5s ≈ 39μs. And the period of ΦRESET is 9984 μs. For such period designs, the output rate would be 100.16 samples per second, which fits the requirement just alright. The delay before di and is right 19.5 μs so that the result of the comparator will control the switches in next phase.

Then, we show the schematic view of this ADC, in which S1, S3 are changed into transmission gate to obtain good performance on both pulling voltage and down (Acharyu *et al*., 2003). However, because S3 and S6 are connected to ground, they do not need to pull the voltage up, so they are built by an NMOS transistor. Similarly, SR is connected in an alternative way so that it can be complimented using an NMOS as well. On the contrary, S5 only needs to pull voltage up, so it is built by a PMOS transistor. Due to this, the signal to control S5 is opposite from the ideal model, say 1 results in S5 open and 0 results in S5 closed. So S4 is eliminated and one AND gate, one OR gate, one NOT gate are used to control S5 and S6. In this way, when it is in phase 1, say Φ1, the gate voltage of S6 is low due to the AND gate so S6 is open, the gate voltage of S5 is high and S5 is open too. In phase 2, when di is low, is high, the gate voltage of S6 and S5 are both high, so S5 is open while S6 is closed and when di is high, is low, similarly, the gate voltage of S6 and S5 are both low, so S5 is closed while S6 is open.

The main advantages of this ADC include (Chen *et al*., 2012; Ho *et al*., 2012):

- It only needs simple analog and digital circuitry
- It is built by first order integrator so that decoding is not complex either
- There is no need of very precision component. Because only a few components are needed and most of them do no consume large amount of power, the area and power are also very modest
- This very design is even simpler: It only requires 6 switches instead of 7. Most control is completed by logic. Also, di is eliminated so that the complexity is further reduced

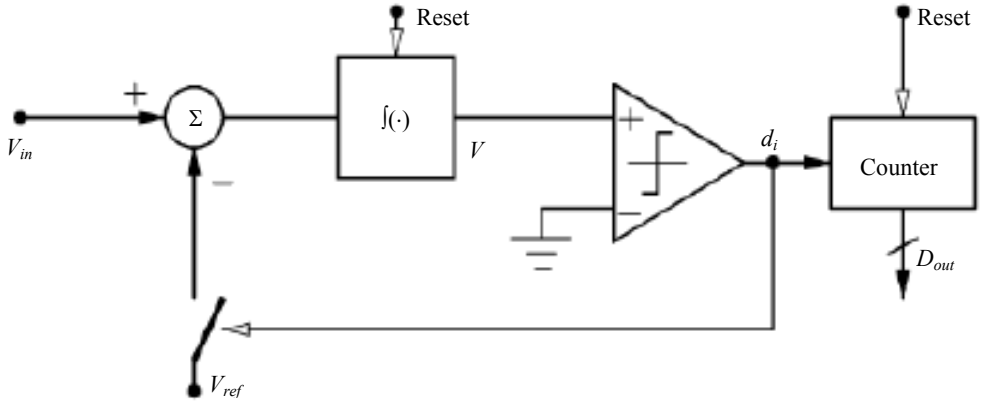

Fig. 1: First-order ADC

However, this incremental ADC suffers from what most incremental ADC do, say it needs a long time (2n clock cycles for n-bit) for each conversion. If higher output data rate needs to be achieved, then this design might not be very suitable (Li and Pun, 2014; Li *et al*., 2014).

The final view of the ADC in Cadence is shown in Fig. 2. It is noted that before the counter, an AND gate is used to connect one clock phase Φ1 and the output of the comparator and then provide input to the counter (PCA/DC, 2012). The usage of this AND gate is discussed in 8.2, part (c). The RESET output node of the counter is not used here. In fact, it is used to generate reset clock in the clock generator. Detailed design of clock generator and counter will be introduced in section 4 and section 8.2, part (b), respectively. NOT gate that converts di into also provides a delay of 19.5 μs.

Capacitor Value

It can be seen from Fig. 2 that the integrator is a non-inverting first-order switched-capacitor integrator, which has a transfer function of the gain of this integrator which we do not need. So C1 and C2 are both set equal to C. In this design, the switched- capacitor integrator contributes most of the noise. For this 1st-order integrator, the opamp is an ideal one. So the noise source is the switch-capacitor part (Pun *et al*., 2013).

During Φ_1 high: Resistance of switch S1 (RonS1) produces a noise voltage on C with variance. And the corresponding noise charge is Q2 = C2V2 = C2kT/C = kTC. During Φ_2 high: Resistance of switch S2 contributes to an uncorrelated noise charge on C at the end of Φ_2, also with a variance. Mean-squared noise charge transferred from V_{IN} to V_{OUT} per sample period is Q2 = 2kTC. In order to keep the noise of the circuit, smaller than 0.5LSB, while 1LSB = Δ3.90625 mV, assuming α = 2 as input referred noise, which is the minimum value of capacitor for this circuit.

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise (Sun *et al*., 2015), which if we assume it is a Nyquist rate ADC. Then we would have that the minimum C is 3.20fF. Of note, the calculation on noise is not adequate accuracy, it depends on the whole noise performance of the integrator including the noise from the switches and the op-amp itself.

However, the minimum capacitor value is mainly determined by the thermal noise requirements (Sun *et al*., 2014a). Thus, the capacitor value in this project is selected to be 10fF in order to provide sufficient accuracy and reduce circuit area and cost.

Detailed Switch Design

The operation principle switched-capacitor integrator whose charging/discharging time constant is 2RonC1 is shown in Fig. 4, where assuming NMOS transistor to be switch.

Theoretically, knowing that the voltage drop caused by closing a transistor switch, we can yield the figure of merit (Sun *et al*., 2014b).

The above equations imply that when L is small, is small, so is ΔV. So in order to have small FOM, minimum L is preferred, which also helps save area. Also, for switch charge injection of slow switch application, where is the overlap capacitance and equals to $L_D W C_{ox}$. So a smaller L can also reduce ΔV. However, when L is too short, it is possible to cause short-channel effect and affect the performance. So in this project, L of all transistors is chosen to be 1.2 times the minimum length, say 1.2×130 ≈ 160 nm.

DOI: 10.3844/ajeassp.2018.611.631

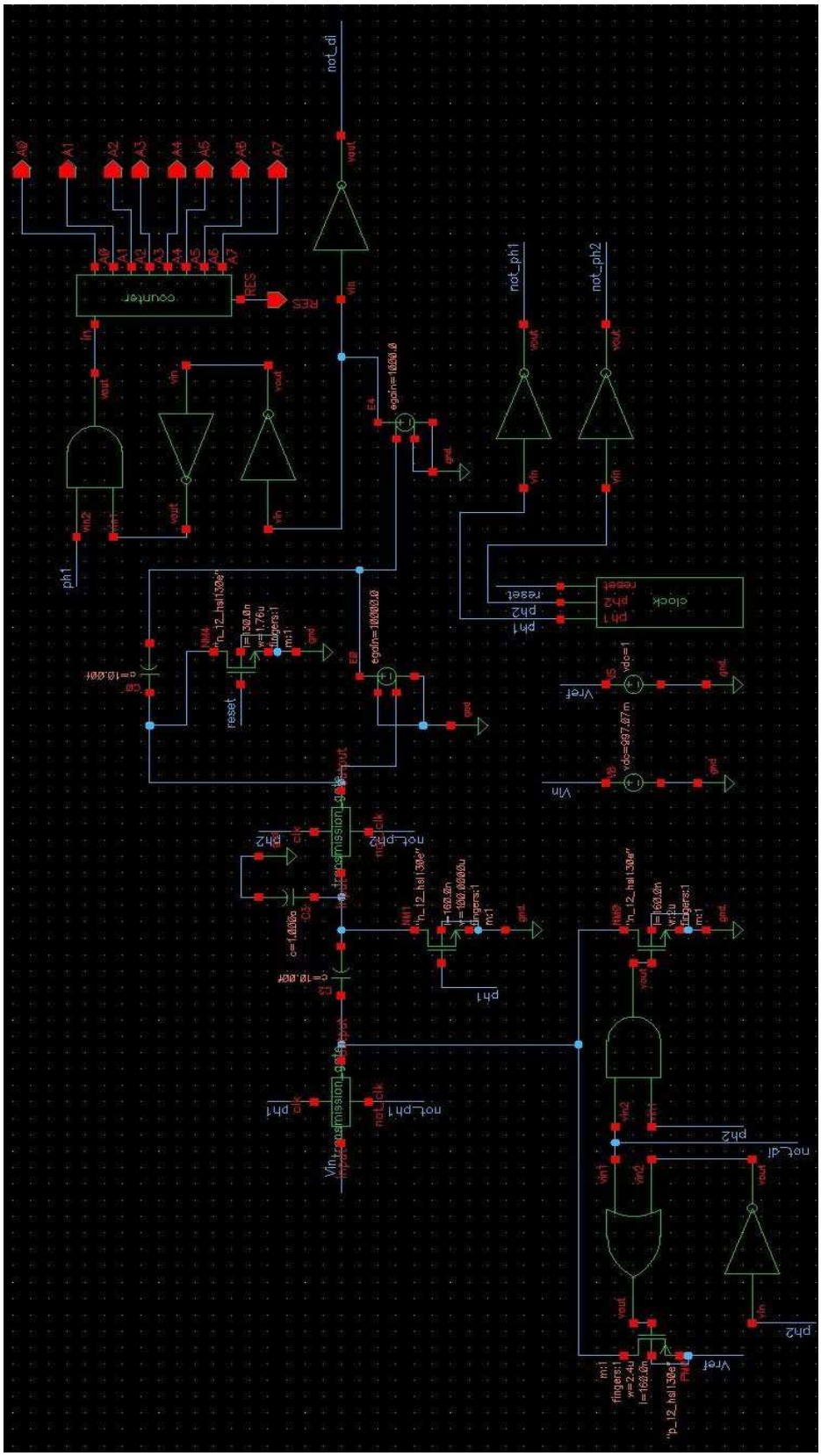

Fig. 2: Cadence view of the ADC

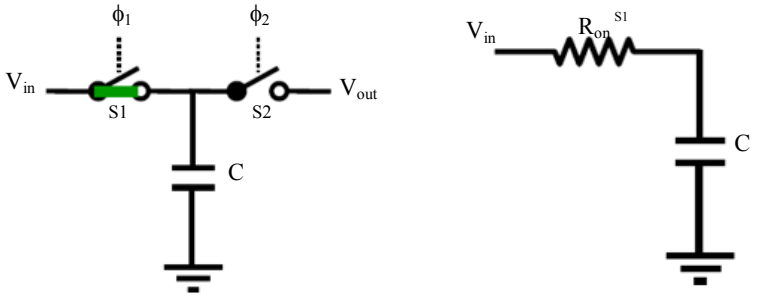

Fig. 3: Switch capacitor

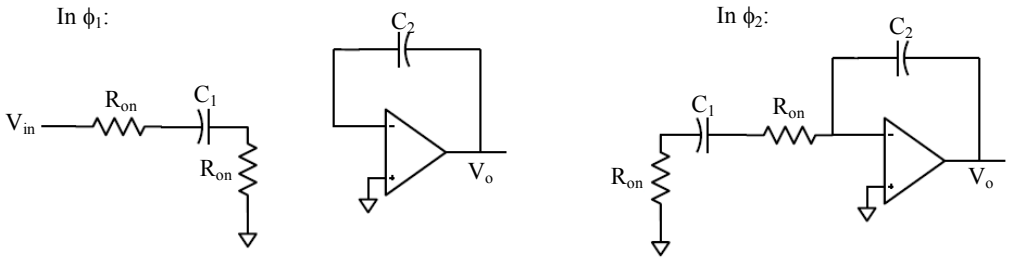

Fig. 4: Operation of a switched-capacitor integrator

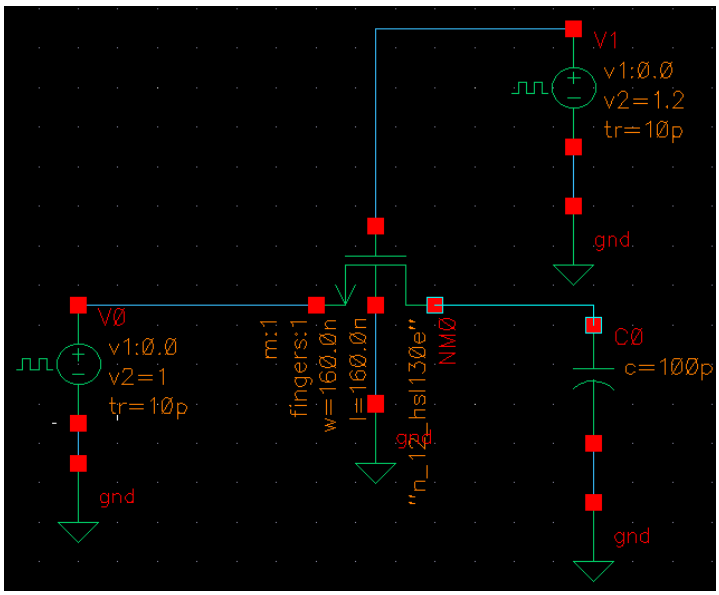

Fig. 5: Simulation of NMOS Switch

Assume we need the voltage across the capacitor to be 99%V_{in} within 100ps in our integrator.

Then from where t = 100 ps and C = 10fF, we can derive that R_{ON} = 2.17 kΩ. Recalling Fig. 3, S_3 and S_6 are NMOS. The worst case for an NMOS switch in this project is when the input voltage connecting to the source of the NMOS is 1V, which results in highest R_{ON} for a given W/L ratio. The performance of an NMOS switch with W/L = 1 (Fig. 5) is simulated. The input is set to be 1V after 2 µs delayand then after another 8 µs, gate voltage will be set to 1.2V. Transient result of the voltage at the top plat of the capacitor within 500 µs is shown in Fig. 8. It is observed that for this very circuit, RC time constant τ = 11.56-10 = 1.56 µs.

Since R_{ON} is proportional to L/W according to the W/L ratio should be 15600/2170 = 7.2. Therefore W_n for this case should be 1.15≈1.2 µm so that W/L = 7.5. As for PMOS transistor, it is known that $|\mu_n| \approx 2|\mu_n|$. So W_p should be $2W_n$ = 2.4 µm to achieve similar R_{ON}.

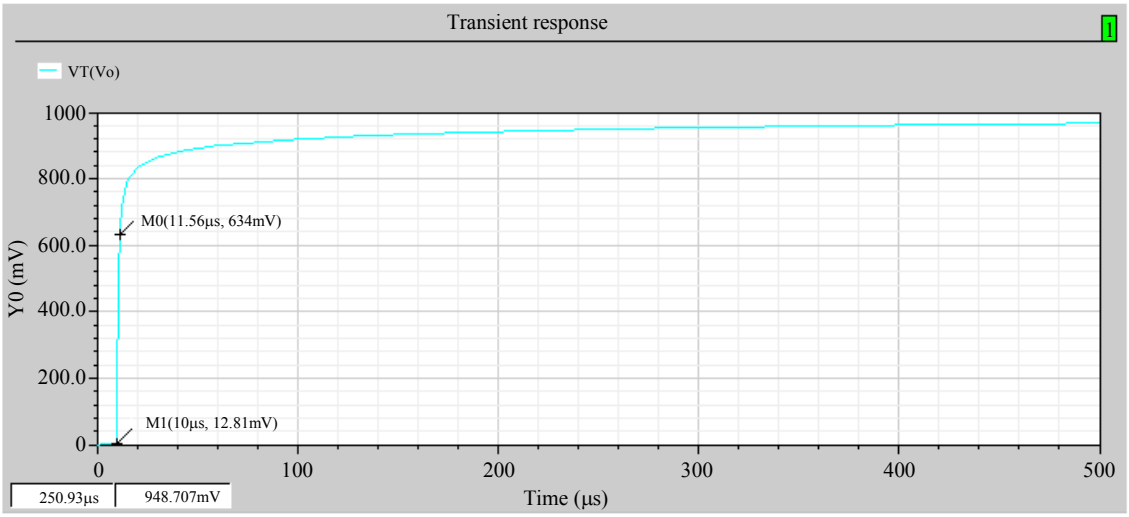

Fig. 6: Output voltage of the switch

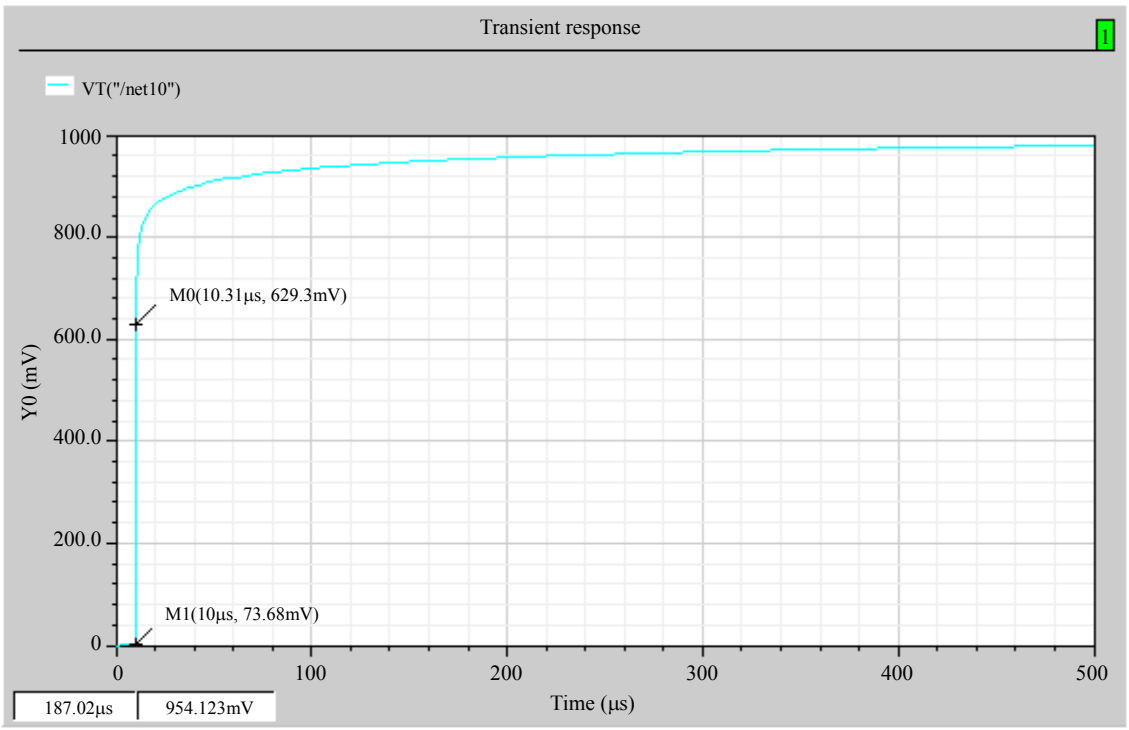

Fig. 7: Output voltage of NMOS with W/L = 7.5

Based on previous calculation, the NMOS transistor with calculated W/L ratio is simulated and the result is shown in Fig. 6. However, it is seen that τ = 0.31 µs so R_{ON} = 3.1 kΩ. By increasing the W/L ratio from 7.5 to 11, R_{ON} reaches wanted value (result shown in Fig. 10).

Nevertheless, when performing PMOS simulation, with a W/L ratio = 15, the performance of the PMOS is almost as good as the calculation, shown in Figs. 7-9. We can see that for this PMOS, τ = 0.19 µs, which means that RON = 1.9 kΩ. In this designed ADC, there is no "worst case" for PMOS to suffer. For S1 and S2, when VS of PMOS becomes small enough, NMOS will dominate so PMOS does not suffer and for S5, VS is constant 1V.

As for transmission gate S1 and S2, since NMOS performs good ability to pull voltage down while PMOS performs good ability to pull voltage up, the worst case

DOI: 10.3844/ajeassp.2018.611.631

for a transmission gate is about 0.5V, as shown in Fig. 10, although this worst case point is varied with respect to the relative difference between the two transistors' W/L ratios.

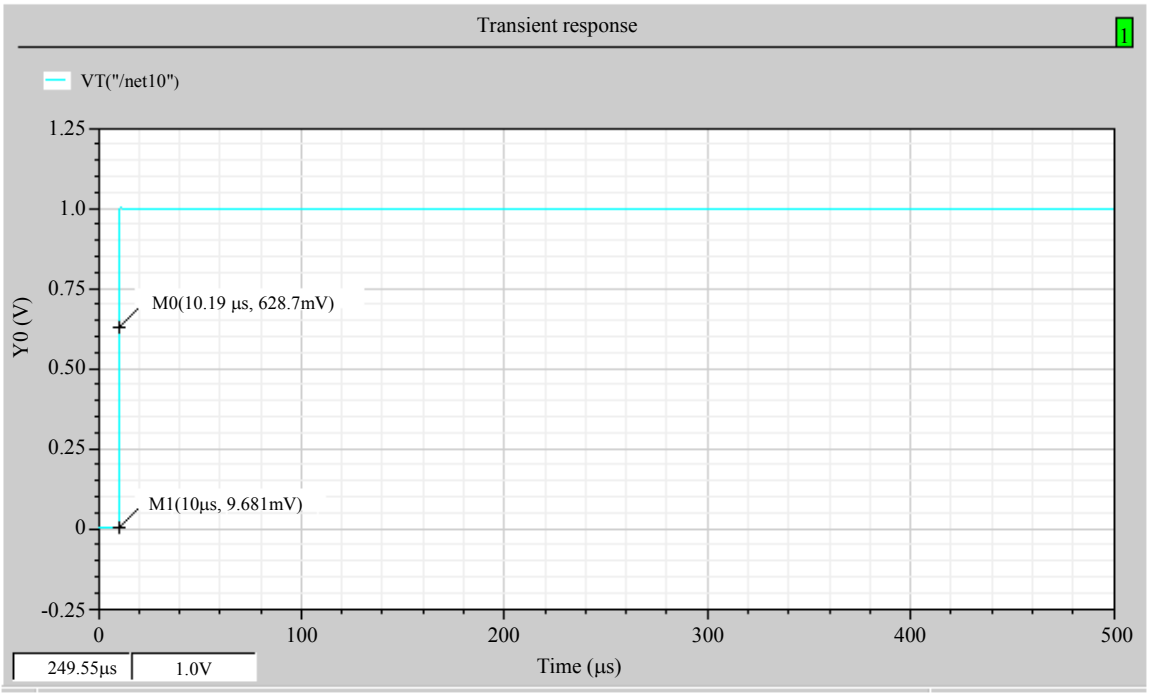

Fig. 8: Output Voltage of NMOS with W/L = 11

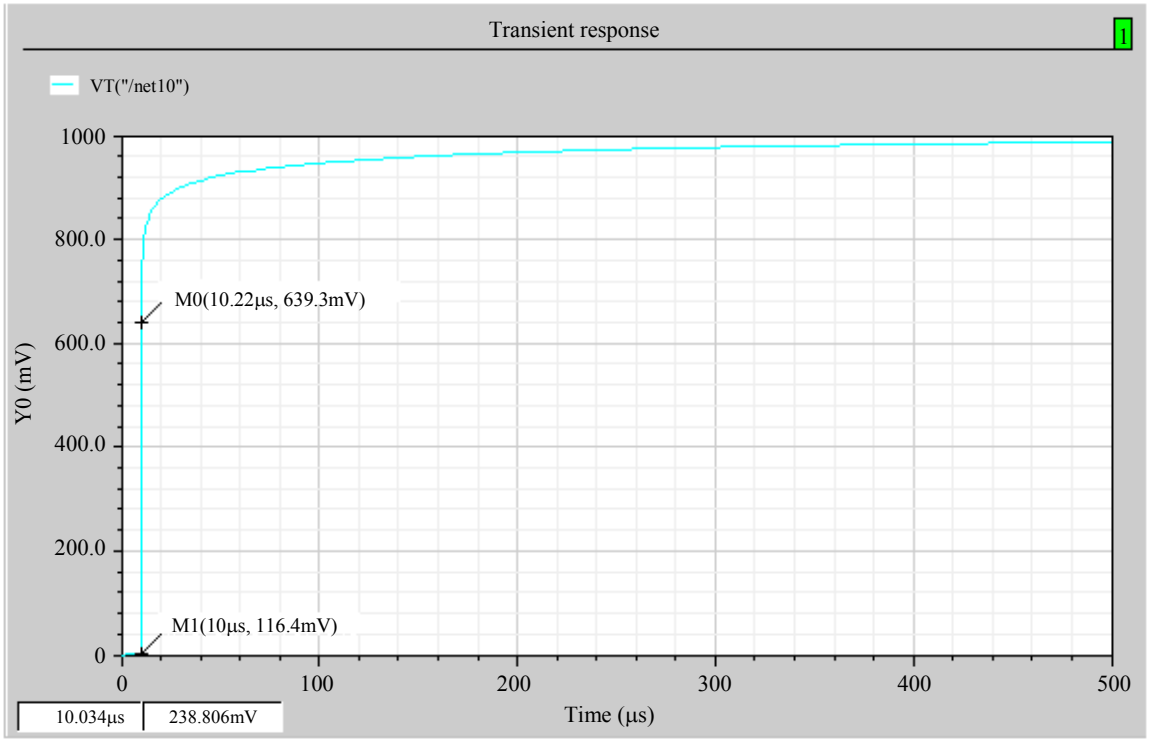

Fig. 9: Output voltage of PMOS with W/L = 15

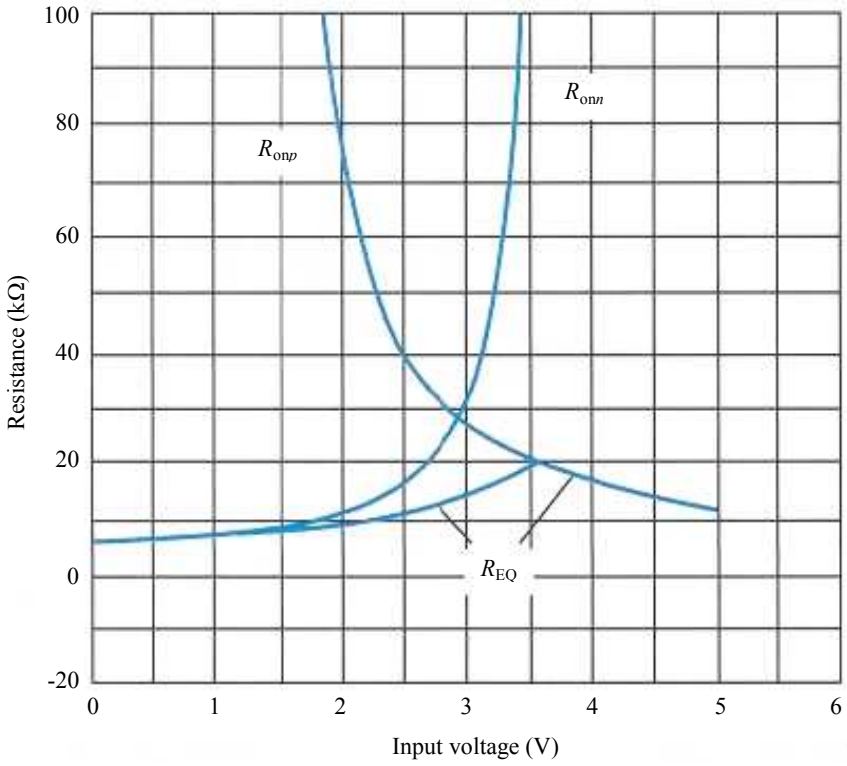

Fig. 10: Resistance of transmission gate

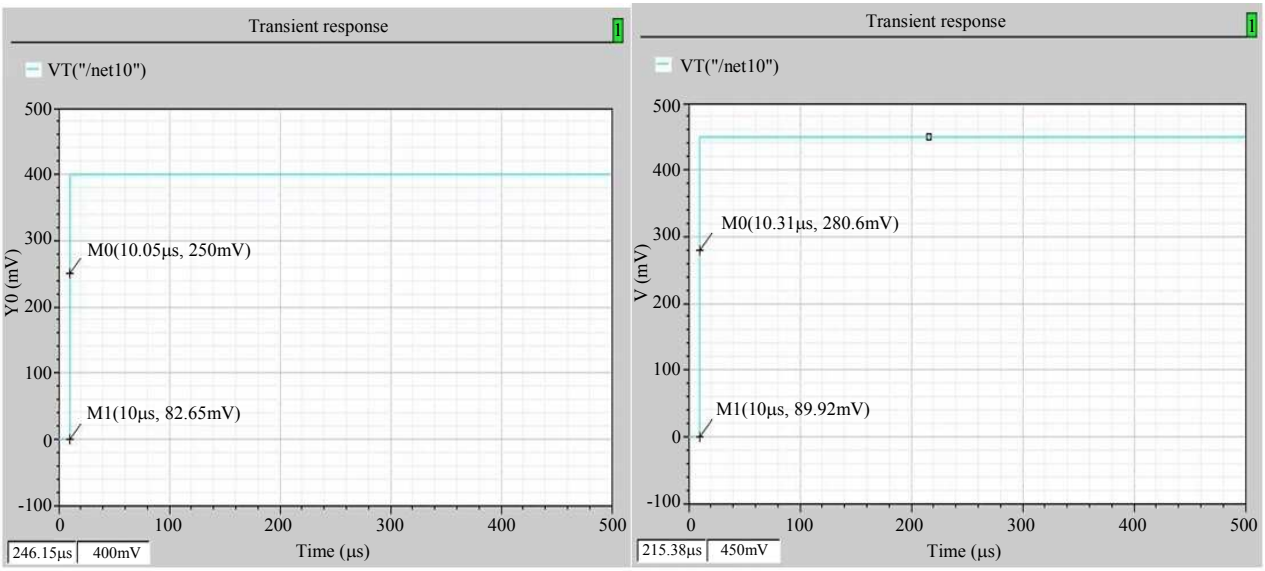

Fig. 11: Simulation of RC Constant for different V_{in}

If we set the NMOS and PMOS inside transmission gate to be the same as previous value, say 11 for NMOS and 15 for PMOS, the transmission gate is simulated with different Vin including 400 and 550 mV. The result is shown in Fig. 11.

We can see that even the worst case among these four has only 31 µs RC time constant which suggests that R_{ON} = 3.1 kΩ. Considering the original assumption is to make the voltage across the capacitor reach 99%V_{in} within 100ps, the performance of the transmission gate is quiteacceptable. Inaddition, the RESET switch of the integrator does not have much requirement since it just needs to discharge C_2 within half of sampling clock period, so its W/L ratio can be smaller to save area. Here

DOI: 10.3844/ajeassp.2018.611.631

we assume it has the same W/L ratio as the other NMOS for easier manufacture.

Clock Circuit Design

Assuming clock Φ_1 is given, what we need then is Φ_2 and Φ_{RESET}. Using NOR gate, NOT gate and feedback with delay can help us get Φ_2 that is non-overlapping with Φ_1. And the counter can count the pulses of Φ_1 and then returns Φ_{RESET} when the counter counts to 11111111 (255).

The delay to get Φ_2, DELAY, in the gate circuit part is 200 ns, while the delay to get Φ_{RESET}, DELAY_C, is 39 µs in order to make Φ_{RESET} high after a complete conversion cycle instead of when right after the counter gives 11111111 at its output put. The AND gate before Φ_{RESET} is necessary because the counter only generates pulses with 39 µs pulse width while for reset we need 19.5 µs pulse width. So this AND gate eliminates the latter half pulse width with the help of Φ_1 which is high initially after 256 cycles and then low after another 19.5 µs and can therefore drive Φ_{RESET} low.

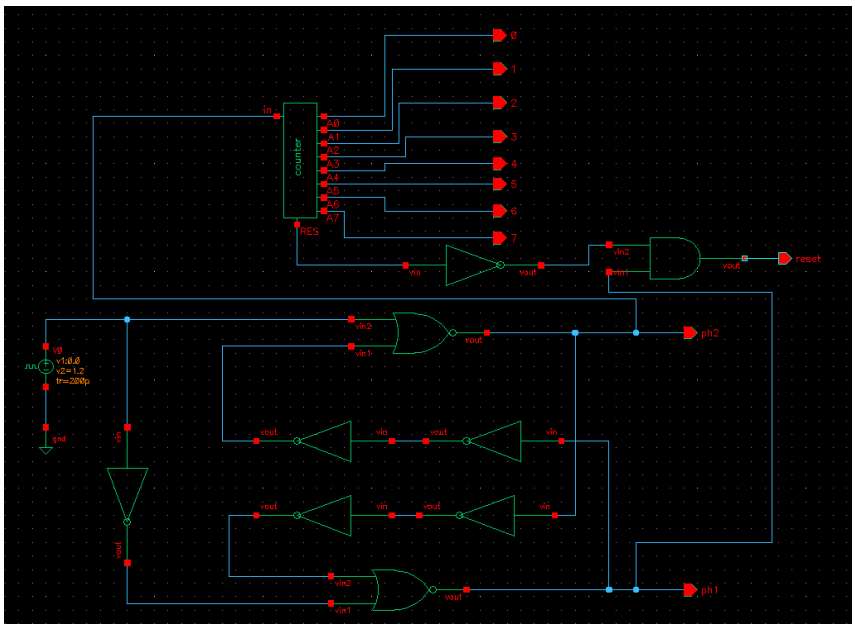

Fig. 12: Clock Generator Schematics in Cadence

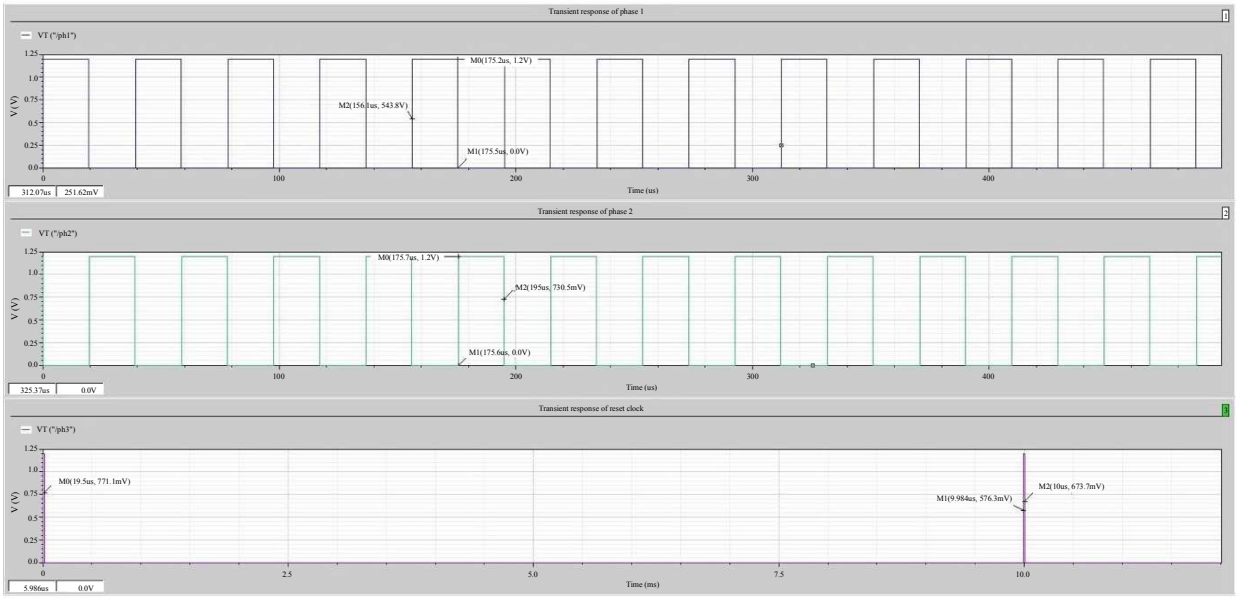

Fig. 13: Output wave forms of the clock

However, this clock lacks an initial pulse at the beginning. A good and practical way is to use the counter's reset clock. Detailed counter design is given in 8.2, part (a). Figure 12 gives the view of the clock circuit in Cadence. And Fig. 13 gives the output waveform of this clock generator. It can be easily seen that Φ_1 and Φ_2 are non-overlapping opposite clocks and Φ_1 is initially be high. Φ_{RESET} has a period of 9984μs and the pulse width of it is 19.5μs. The output of the counter A0 to A1 is useless in this clock generator and can be omitted.

Output Examples

Input Near 0

It is chosen that the input voltage is 117.7μV. Figure 14 shows the first 4 digits of the ADC and Fig. 15 show the latter 4 digits throughout the whole sample period (9.984ms). It is clear that after the first half cycle of Φ_1, all digits except A0 are 0. So the output of this ADC under the circumstance of 117.7 μV input voltage is 00000001 (1). Figure 16 shows the waveforms of the outputs of the comparator and the opamp.

Input Near $V_{ref}/2$

It is chosen that the input voltage is 507.1727 mV. Figure 17 shows the first 4 digits of the ADC and Fig. 18 show the latter 4 digits during the last switch clock period, say from 9945 to 9984 μs. It is clear that, in the end, all output nodes of the ADC other than A0 and A7 are low. So the output of this ADC under the circumstance of 507.1727mV input voltage is 10000001 (129). Figure 19 shows the waveforms of the outputs of the comparator and the opamp.

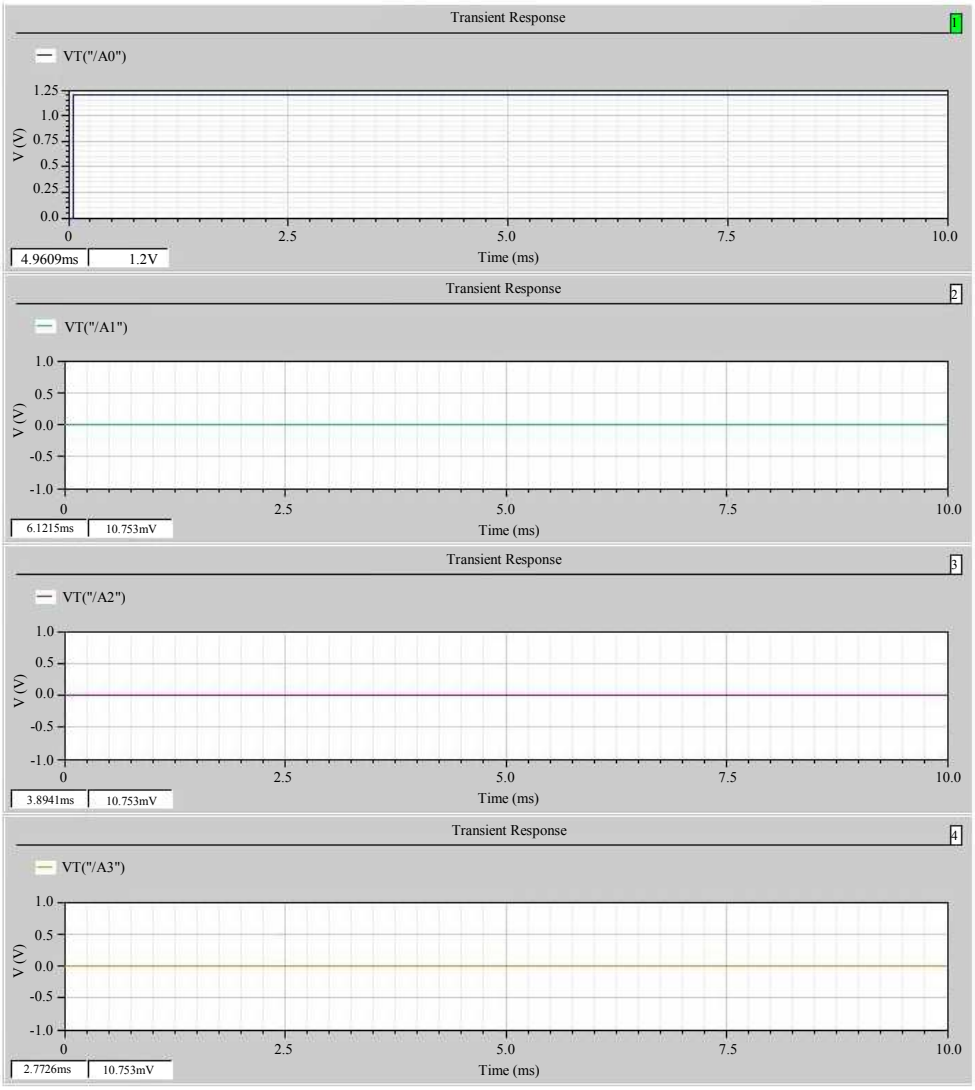

Fig. 14: First 4 digits of the ADC (A0, A1, A2, A3)

DOI: 10.3844/ajeassp.2018.611.631

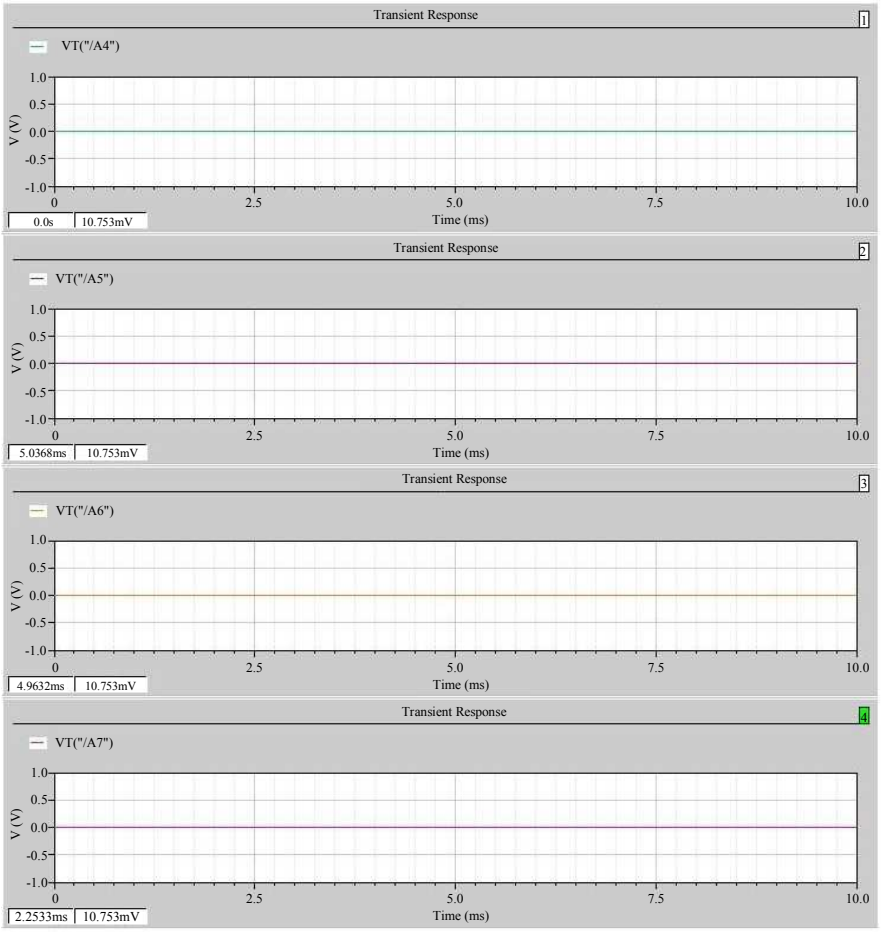

Fig. 15: The rest digits of the ADC (A4, A5, A6, A7)

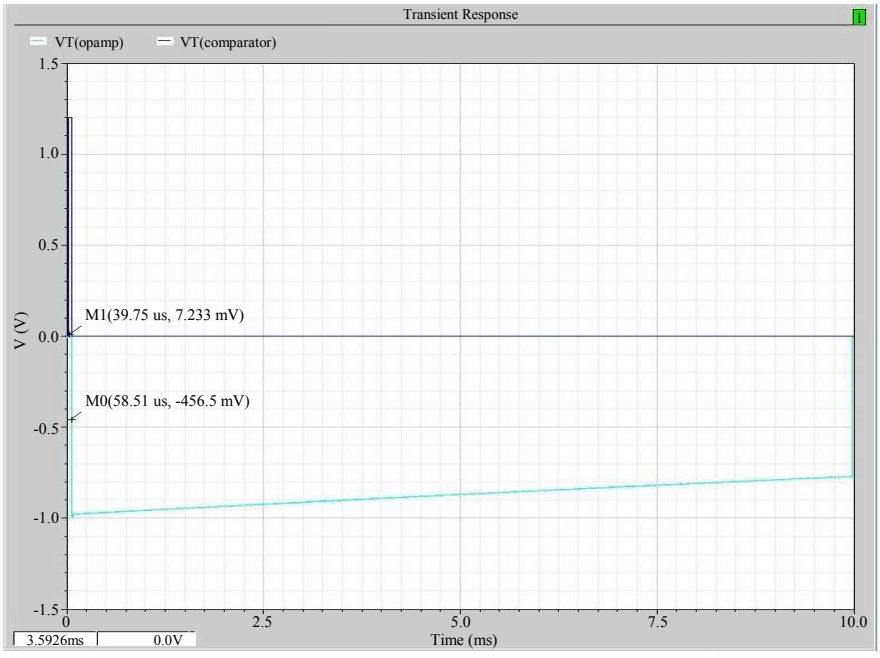

Fig. 16: Output Waveforms of the Opamp and the Comparator

DOI: 10.3844/ajeassp.2018.611.631

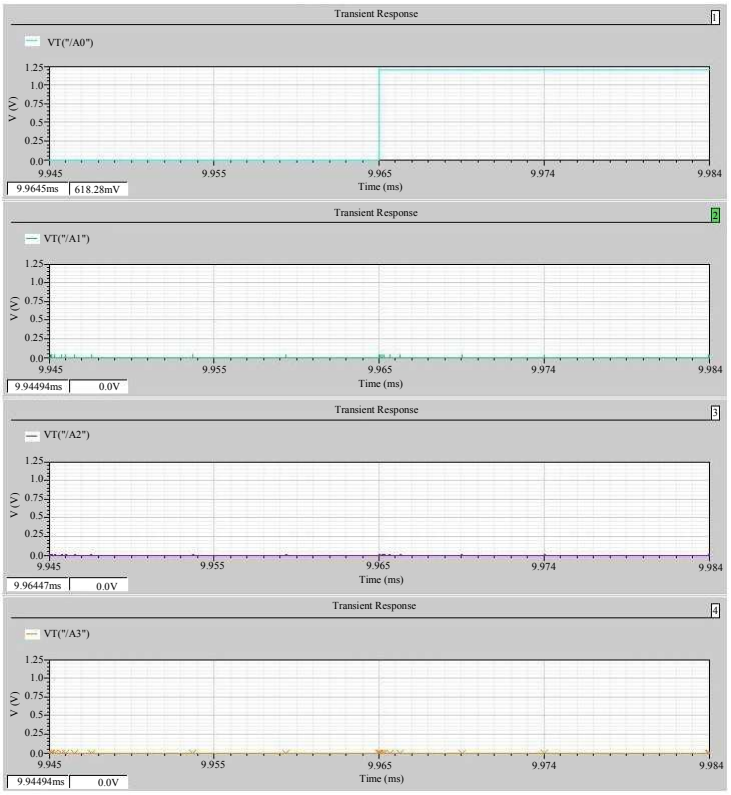

Fig. 17: First 4 digits of the ADC (A0, A1, A2, A3)

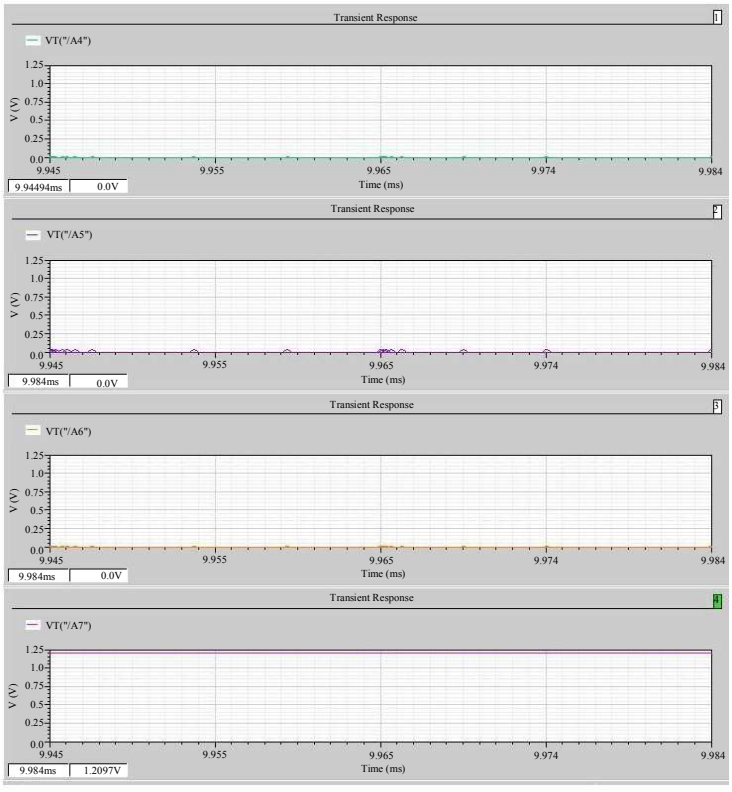

Fig. 18: The rest digits of the ADC (A4, A5, A6, A7)

DOI: 10.3844/ajeassp.2018.611.631

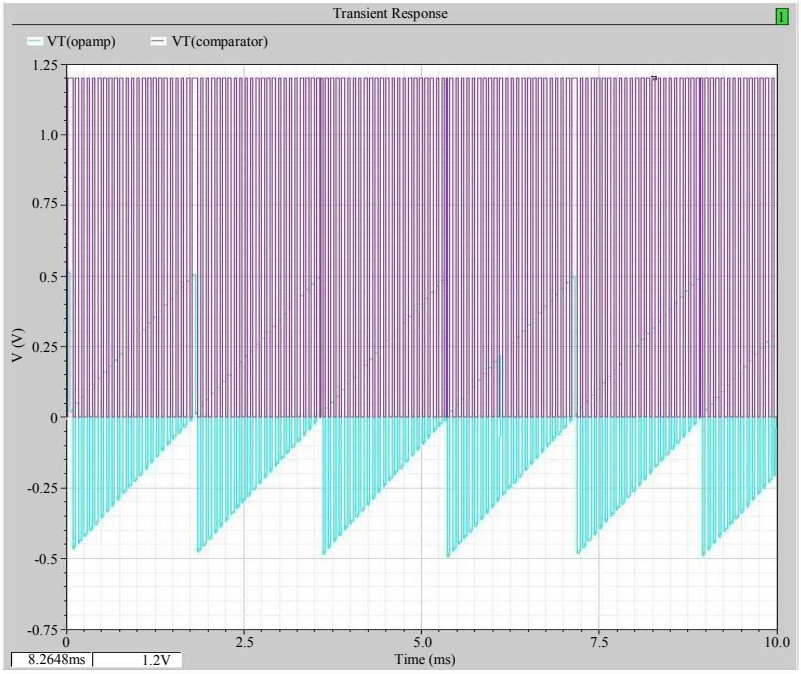

Fig. 19: Output waveforms of the opamp and the comparator

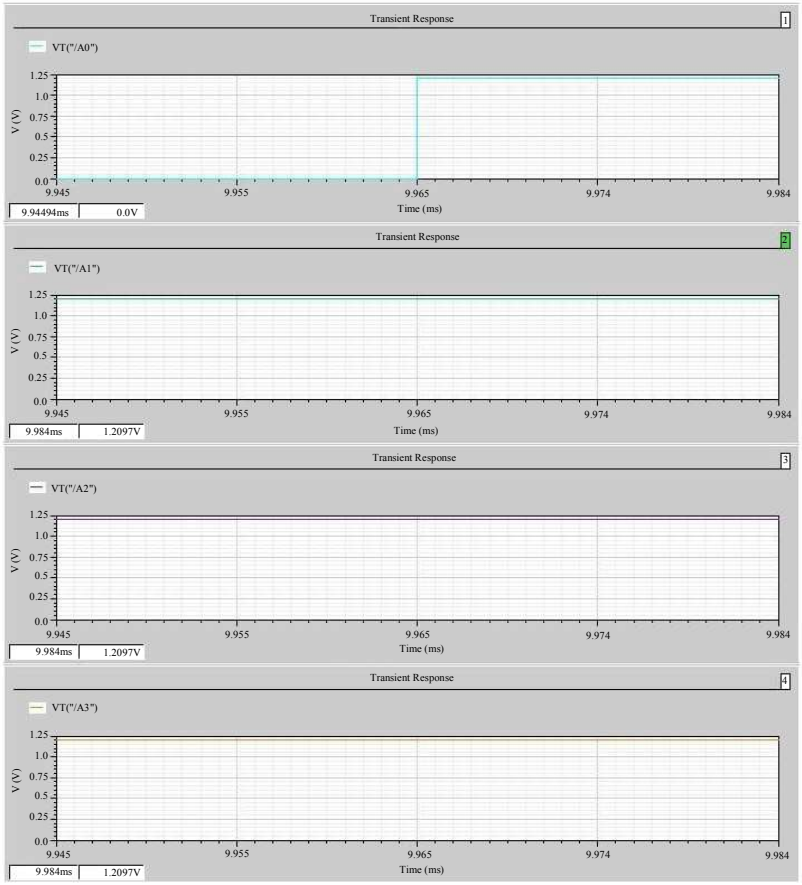

Fig. 20: First 4 digits of the ADC (A0, A1, A2, A3)

DOI: 10.3844/ajeassp.2018.611.631

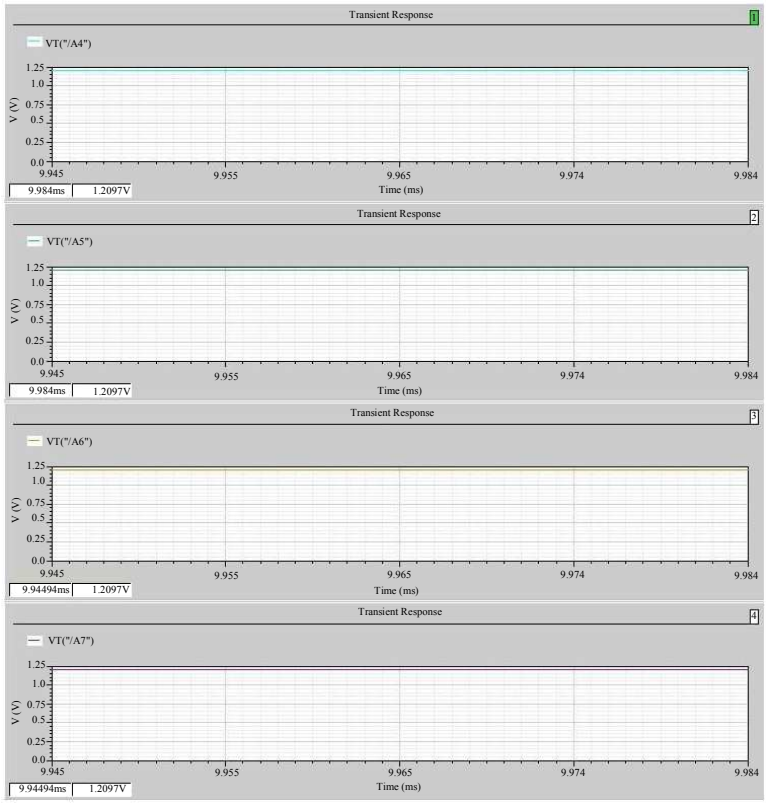

Fig. 21: The rest digits of the ADC (A4, A5, A6, A7)

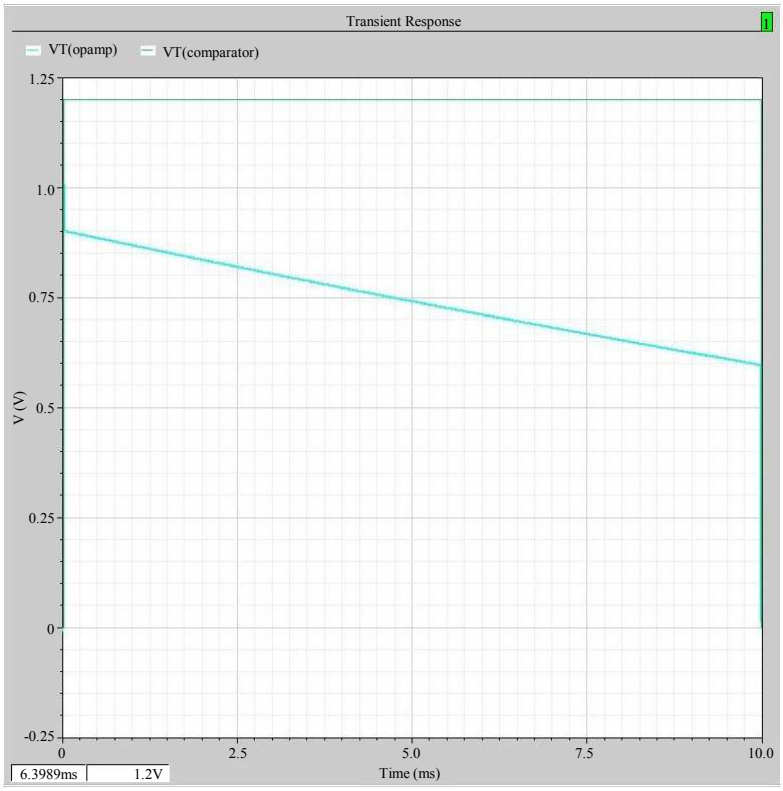

Fig. 22: Output waveforms of the opamp and the comparator

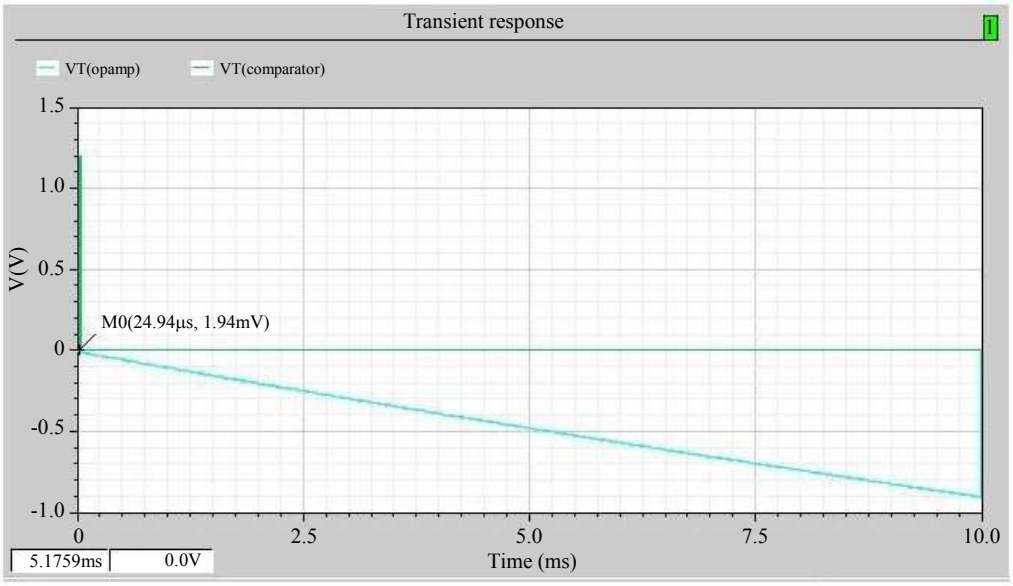

Fig. 23: Output waveforms of the opamp and the comparator ($V_{in} = -\Delta$)

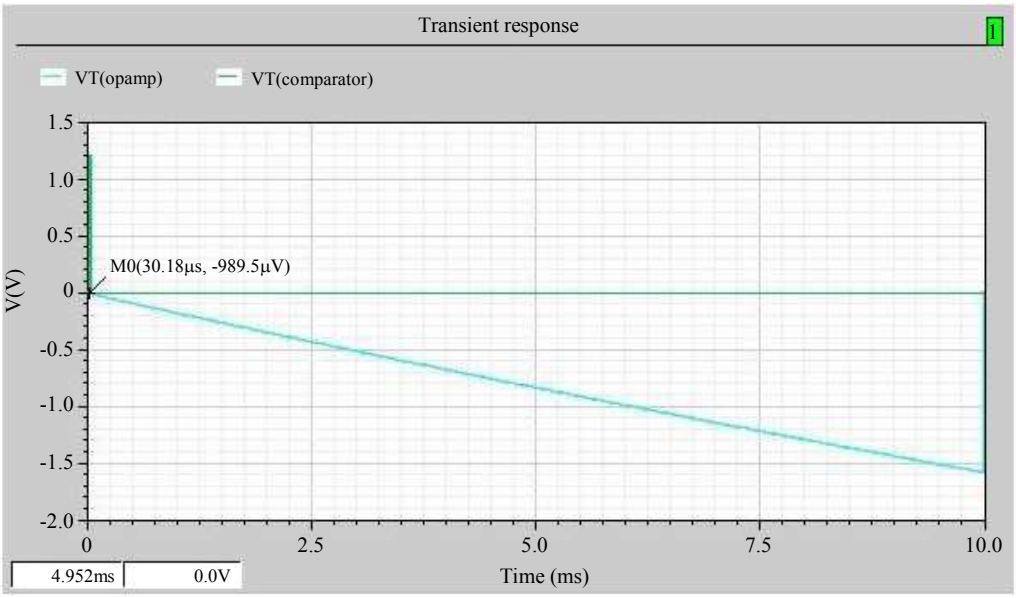

Fig. 24: Output Waveforms of the Opamp and the Comparator ($V_{in} = -1.75\Delta$)

Input Near V_{ref}

It is chosen that the input voltage is 998.979mV. Figure 20 shows the first 4 digits of the ADC and Fig. 21 show the latter 4 digits during the last switch clock period, say from 9945 to 9984µs. It is clear that, in the end, all outputs node of the ADC are eventually high. So the output of this ADC under the circumstance of 998.979mV input voltage is 11111111(255). Figure 22 shows the waveforms of the outputs of the comparator and the opamp, while Fig. 23 shows the waveforms of the output of the opamp and Fig. 24 shows the input of the counter. It is obvious that the output of the comparator becomes 1.2V dc and the signal to the counter becomes pulses with the aid of the AND gate and the clock signal Φ_1. Thus, the counter can count the number of pulses and work properly.

Offset and Gain Errors

Offset Error

In the previous part, it is shown that when V_{in} is about 0, the output of this ADC is 1. And when V_{in} is –

DOI: 10.3844/ajeassp.2018.611.631

Δ, say -3.90625 mV, the outputs of the opamp and the comparator are shown below.

It is seen that there is still a pulse in the beginning and the counter still gives 1 when Vin is – 1.75Δ, the outputs of the opamp and the comparator are shown below, which is almost the same as previous.

And when Vin = –2Δ, the pulse vanishes and the counter can give 0 (shown in Fig. 25).

Gain Error

Previously, the output for V_{in} close to V_{REF} has been simulated and the counter results in 11111111 (255). And until V_{REF} – 0.75LSB = 997.07 mV, the final output of the counter keeps 255 (shown in Fig. 26).

When the input voltage is reduce to VREF – 1LSB = 996.09 mV, the final digital output of the counter becomes 11111110. The output at this moment is shown in Fig. 27.

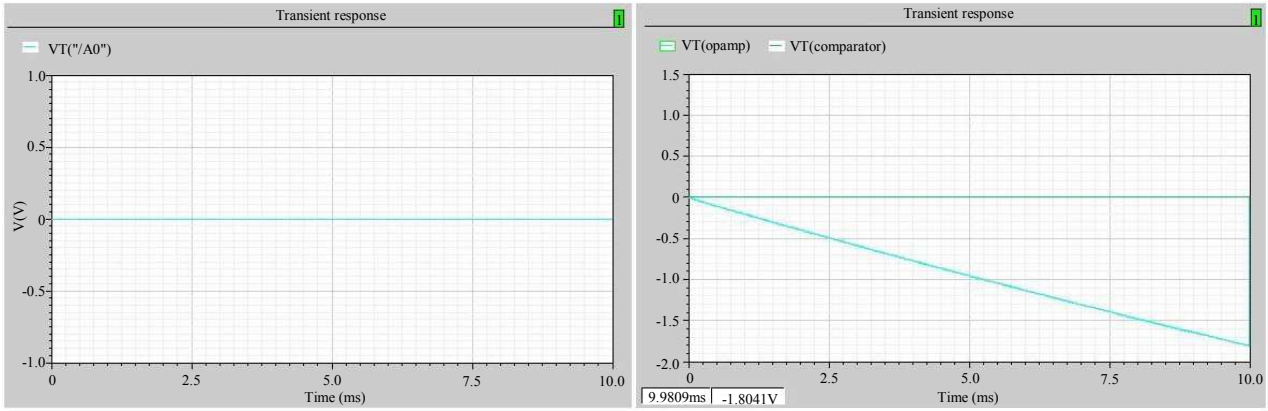

Fig. 25: Output Waveforms of A0 (left), the Opamp and the Comparator (right) (V_{in} = –2Δ)

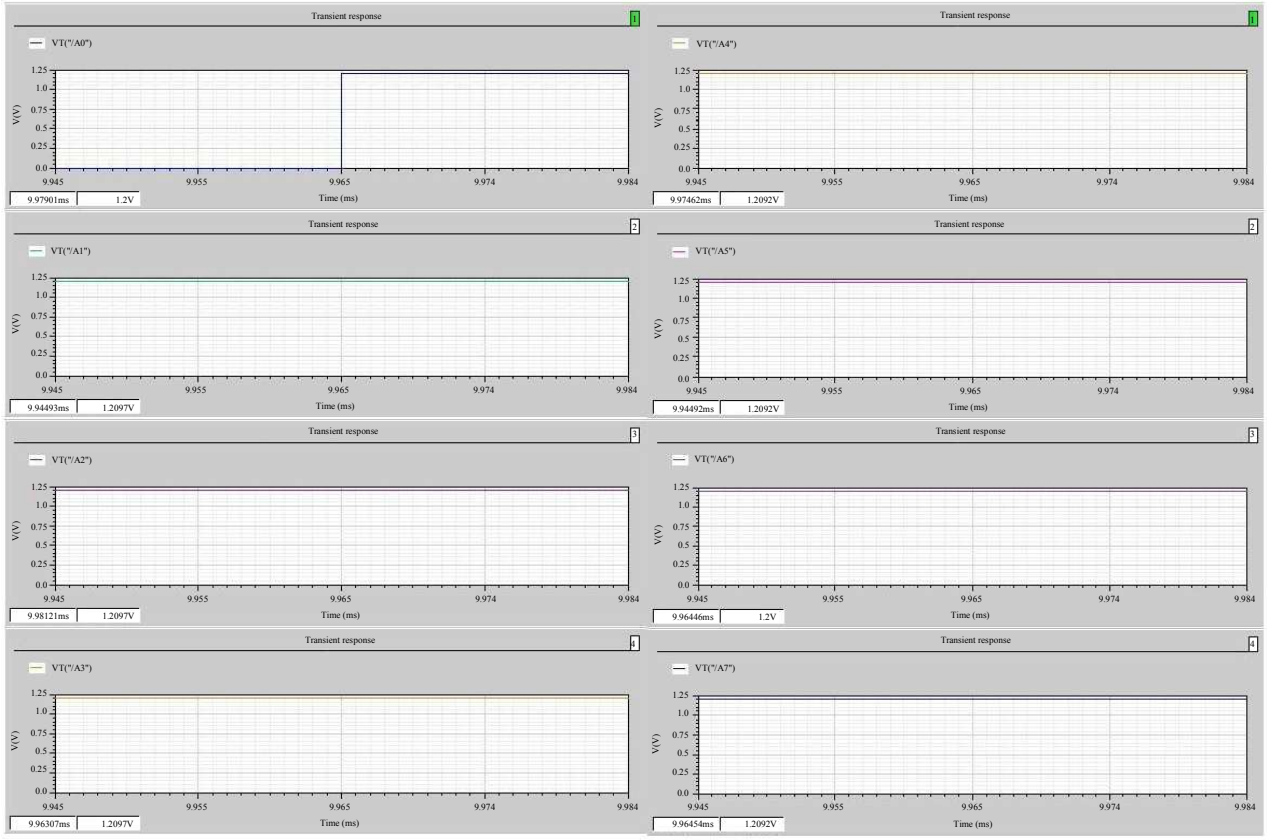

Fig. 26: The output digits of the ADC (A0 to A7) (V_{in} = 997.07mV)

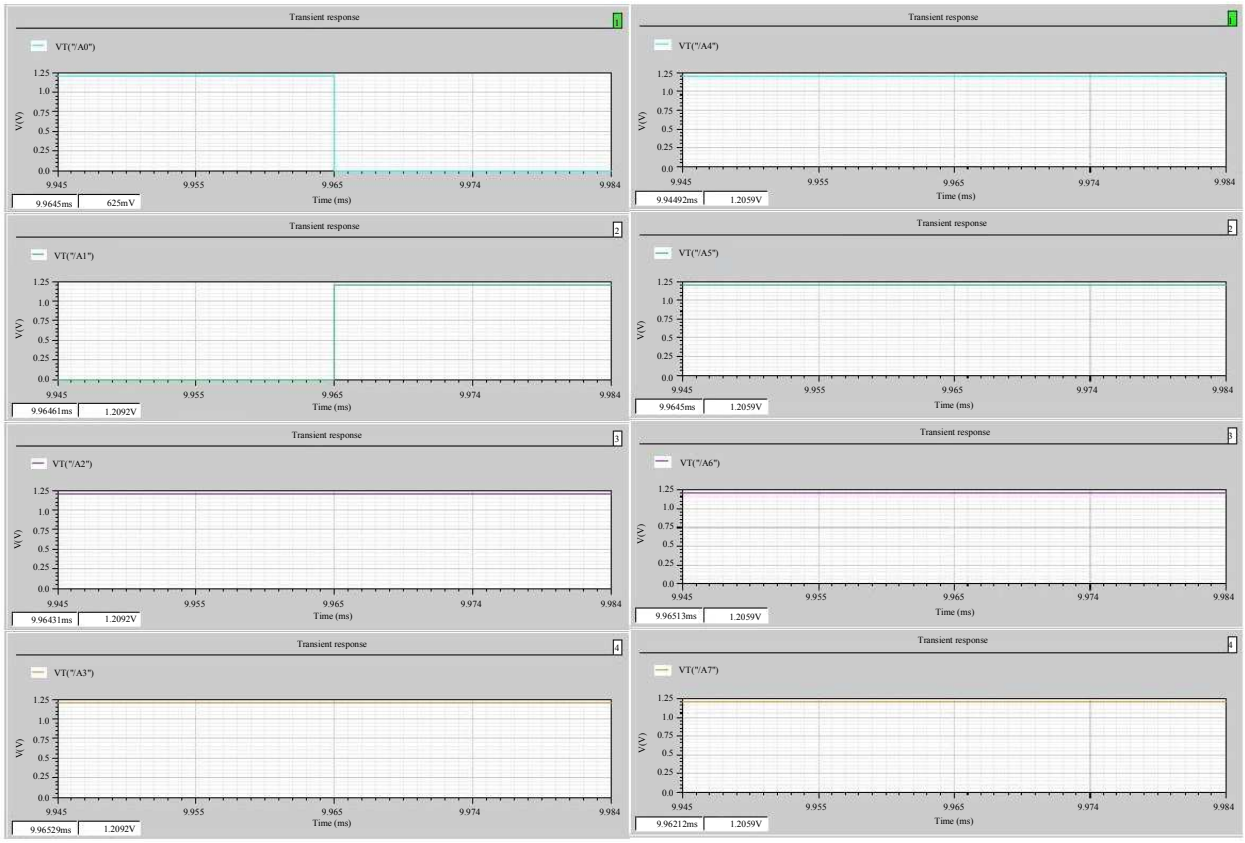

Fig. 27: The output digits of the ADC (A0 to A7) (V_{in} = 996.09 mV)

According to the definition of gain error, which is the deviation of the end point or best fit reference line from the ideal slope of the transfer characteristic, it is equal to the Full scale error with the offset error subtracted.

Causes of Offset and Gain Error

The offset error is caused by the comparator so that when the integrator gives slight minus voltage at its output, the comparator still gives a pulse. It can be eliminated by a small amount of offset between ground and the minus input pin of the comparator though this offset has to be accurate otherwise it will cause positive offset error. Also it can be erased by offset compensator. On the other hand, the reason to cause the gain error is probably switch charge injection. No matter how well it is calculated, there is always a slight ΔV for the voltage across the capacitor, which means that the integrator never truly integrates the real V_{in} but a slightly smaller one for all input value. So the gain decreases causing positive gain error. It is possible to reduce this ΔV using more precisely design switch and/or better technology. Yet in this project, only theory to remove these two errors is introduced. Techniques to cancel these error are for future design.

DNL and INL

In this section, histogram method is used to calculate the DNL and INL of this ADC. The simulating principle is shown in the Fig. 28. To measure the non-linearity, a cosine wave with amplitude from -1V to 1V is used as input.

By counting the numbers of output codes and then the probability of each code to appear, this method can then provide us DNL information from which we can derive INL by integration. The probability of code i is Pi = ti/π, so the threshold level of code i can be used to determine the DNL. The steps needed to derive DNL with corresponding resolution can be calculated. Of note N stands for the number of ADC bits, Zα/2 for the confidence level and β for the DNL resolution in LSBs. Knowing that Common values for the confidence level (Zα/2) are:

- 90%: 1.645
- 95%: 1.96
- 99%: 2.576

We can get that the for a DNL resolution of 0.1LSB and confidence level of 90%, we need 108816 samples for our ADC. Because we just need half of one cosine input period to test all input voltage, for this very sample number, the period of the cosine wave should be 2176.32s.

DOI: 10.3844/ajeassp.2018.611.631

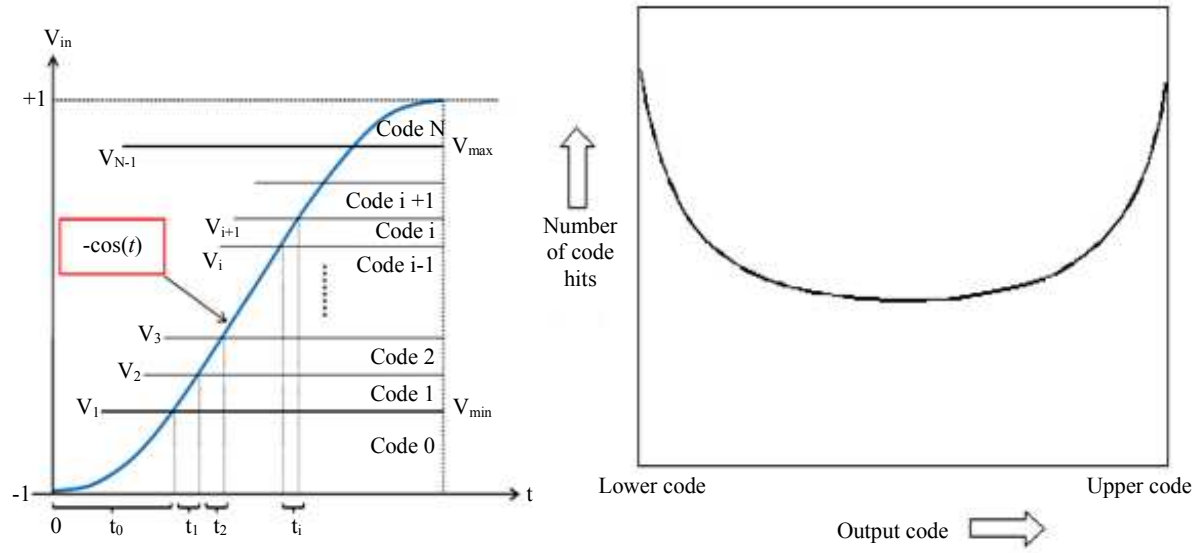

Fig. 28: Histogram method input

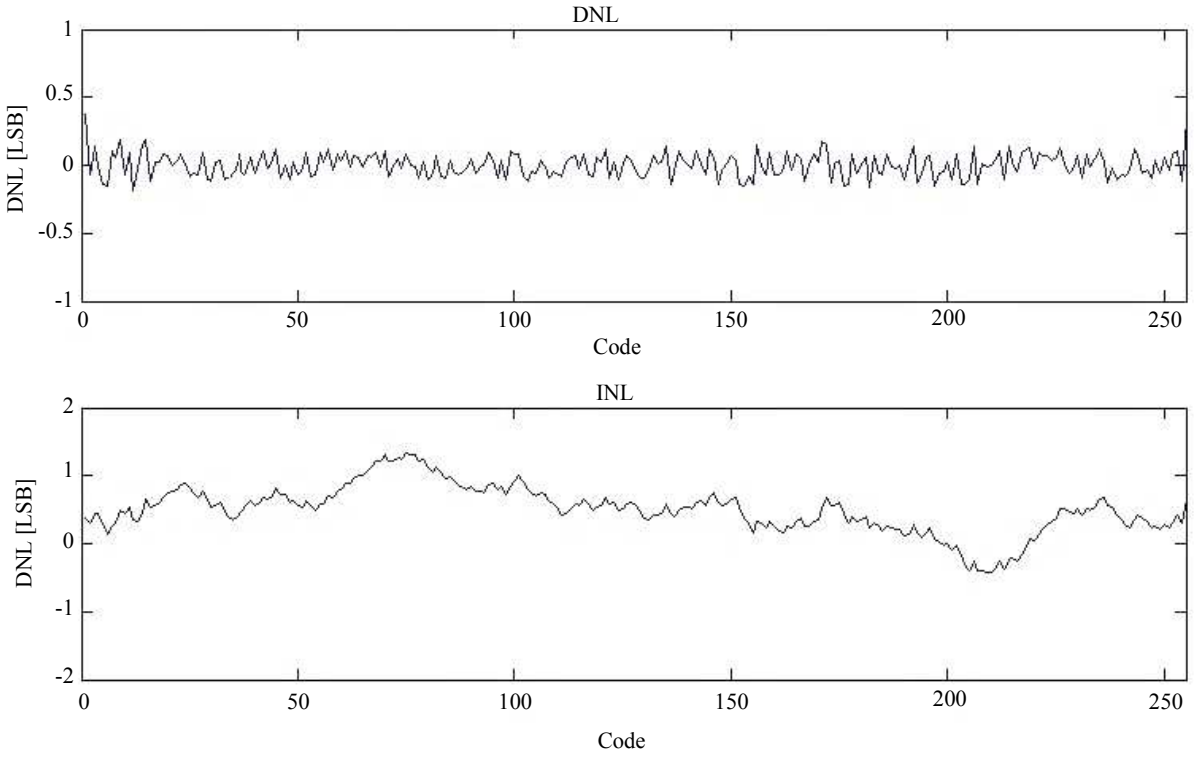

Fig. 29: DNL and INL of this ADC

However, time required for such a simulation is too long. Due to lack of time, only 1700 samples were tested. A clock that is almost the same as the reset clock of the integrator except 39μs time shift ahead of ΦRESET is used to select the final output of the ADC for each conversion cycle. Then the output is forward to an ideal DAC, of which the output is then collected and analyzed using MATLAB. The final result of the DNL/INL analysis is shown in the Fig. 29.

It is noted that code 00000000 is considered undefined and thus removed from the result. Also, because very limited samples were tested and analyzed,

this result is not very accurate. For more accurate result on non-linearity characteristics of the ADC, more simulation time could help.

Discussion

Comparison

An 8-bit incremental ADC with very simple and straight forward design is proposed in this project. It provides the ability to convert analog signal (from 0 to 1V) to digital code (00000001 to 11111111, or 00000000 to 11111111 if negative voltage is input) with an output data rate of about 100 samples per second under 1.2V supply voltage. The design is based on UMC 0.13μm CMOS and logic gates through which the circuit is control by one master clock with all the other clock needed being generated by itself. In this report, several performance parameters are simulated and discussed. Compared with an ideal incremental ADC, this one performs offset and gain errors as well as DNL and INL. One most significant defect is the offset error, due to which, when there is no sufficient negative input, this ADC does not generate 00000000. Apart from that, this ADC basically works properly.

Compared with other types of ADC or some same type ADC, this one is also slower according to the project requirement. Though the speed is able to be shifted higher, it has certain limit. If above the limitation, higher order design might be needed. When the speed requirement gets even higher, another type of design, such as flash ADC or pipeline ADC, might be needed.

Problems Encounter in this Project and Solutions

In this project, the counter is built using 8 negative-edge triggered D flip-flops with reset so that after a conversion cycle, this counter can go back to 0 and count again. However, since the only given clock is assumed to be Φ_1, which cannot be directly used to reset the counter, the reset clock for counter has to be generated by itself (Tang and Pun, 2014).

Solution

In this project, another D flip-flop without reset is used to be the initial reset clock. The Fig. 30 shows the construction of this counter.

At first the counter will be reset be the output of the lowest D flip-flop, which gives 0 at Q. Then, because of the clock goes up and the input at D is 1.2V dc, Q keeps 1.2V. The outputs of the counter are only all high in the last clock cycle. So using 7 AND gate results in a pulse in the end. The AND logic between the inverse of this pulse and the constant 1.2V output of the D flip-flop can then generate proper reset clock with a period of 9984μs. Assuming the NOT gate gives a delay of 39μs, the reset clock will be activated after every 9984μs. Moreover, after a NOT gate, the reset clock of this counter can be used to be the reset clock of the integrator of this ADC as well.

For Reset clock generation for the integrator (Fig. 31), initially, the idea of the reset clock design is to use 7 AND gate to give a pulse when A0 to A7 all output 1 and then after a delay of 39μs, it can trigger the reset switch of the integrator. However, the pulse width of the reset clock of the counter is 39μs and we need the pulse width to be 19.5μs for the integrator reset, like the plot below.

It is observed that the 2nd clock pulse has a pulse width of about 44μs, which is unwanted. Solution: AND logic is used to pull down the latter half of the counter's reset clock pulse. Then the reset clock can be as good as Fig. 6.

Regarding to input of the counter (Fig. 32), when Vin becomes large, it is very likely that the output of the comparator will be pulses with wider pulse width but less pulse numbers (Tang *et al*., 2012). This is because the voltage after subtracting phase is for example, if Vin = 0.9V, then the opamp output will be 0.8V to 0.6V to 0.4V. There will bea long time that the output of opamp is higher than 0 which makes the comparator give continuous high voltage. Since when counter counts, what it counts is how many pulses there are, we need to convert the dc voltage into pulses (Tang *et al*., 2015).

Solution

In this project, an AND gate is used to provide AND logic to the output of the comparator and a clock Φ1 so that wide pulse width signal can be converted to pulses with a period of 39 μs, which means when a pulse has a pulse width larger than 2 clock period, it will be counted every clock cycle.

Major Performance Problems and Solutions

Offset error = -2.5LSB, solution: Comparator with error compensation or offset error compensator.

Gain error = 2.5LSB, solution: Switches with better performance.

Further Improvement

First of all, if permitted with more time, a more accurate simulation of DNL and INL shall be cast as well as analysis on SNDR, ENOB, SFDR and aperture uncertainty. Based on the new accurate DNL/INL result and the other performance parameters, the following parts shall be able to be optimized to improve DNL, INL and so on:

- Switch, both size and type might be further improved
- Comparator, a comparator that can remove offset is of use if it is possible. Or an offset compensator can improve the performance as well

- Opamp design, in this project, an ideal opamp is used, which is not possible in the real case. So an opamp suitable for this very project is wanted
- The whole design could be changed, such as switch controlling method, design of integrator and so on, in order to obtain better performance

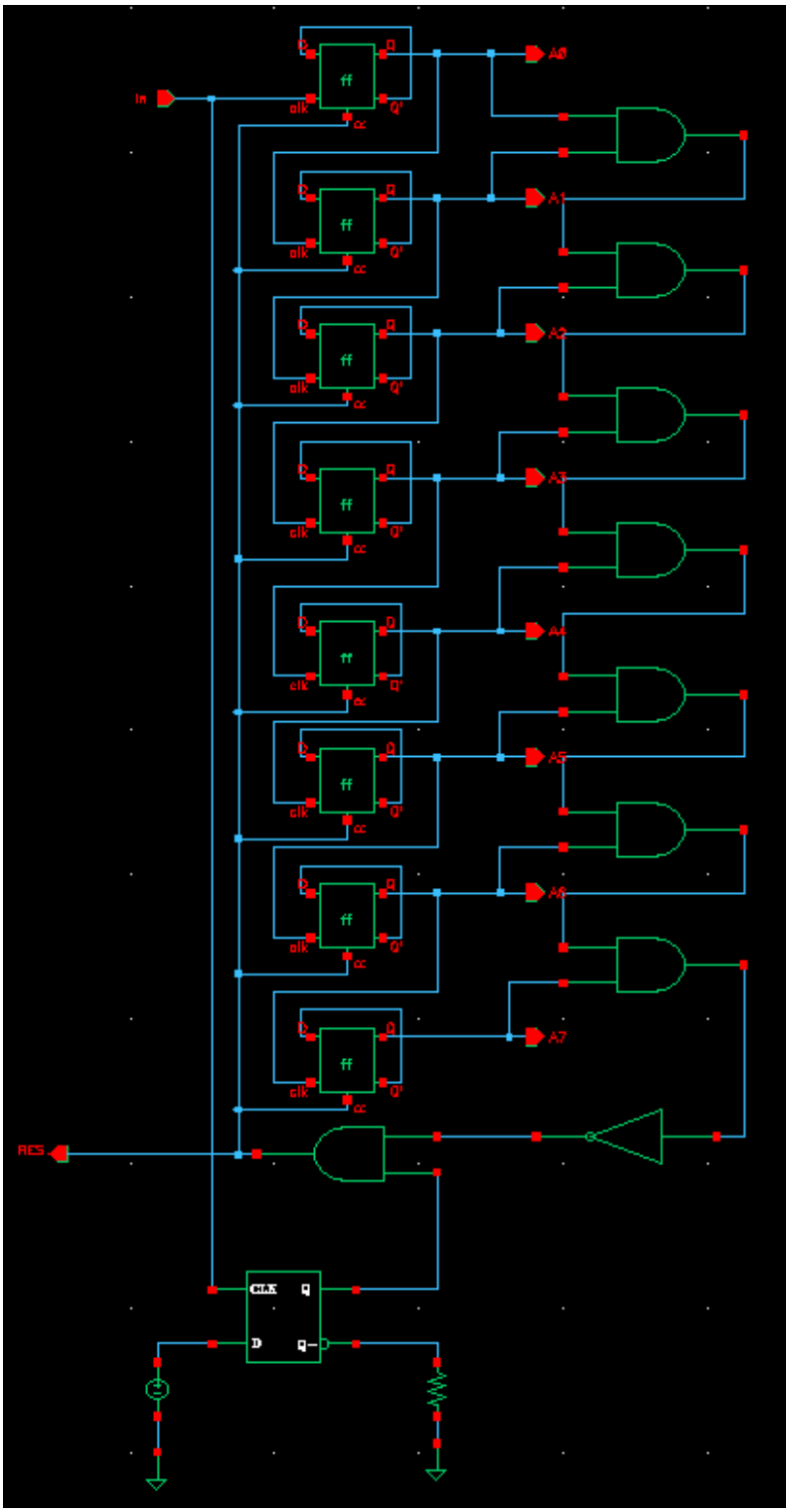

Fig. 30: Schematic of the counter

DOI: 10.3844/ajeassp.2018.611.631

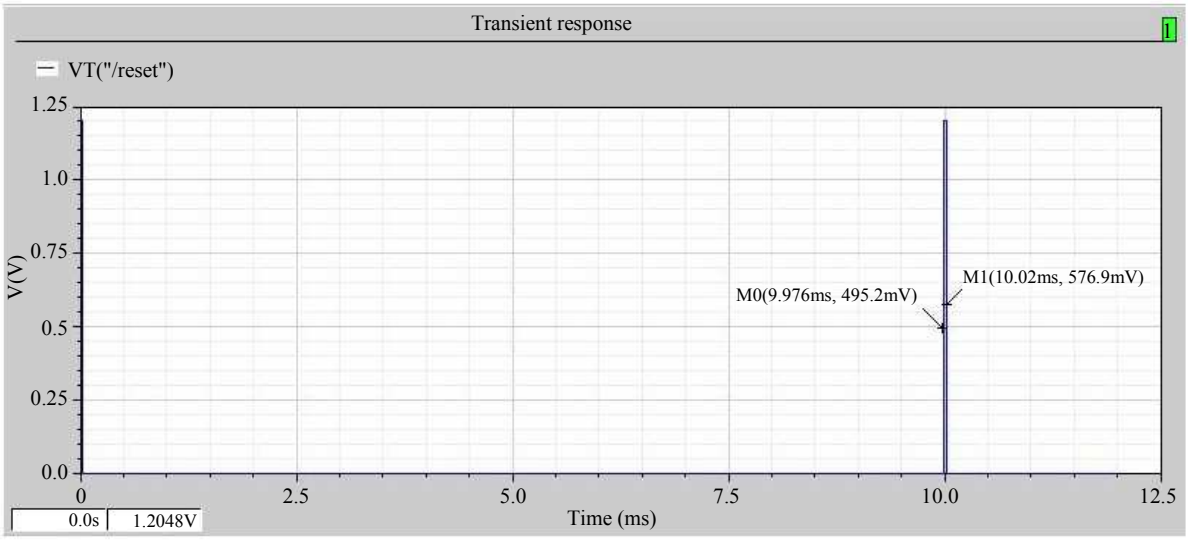

Fig. 31: Reset clock with problem

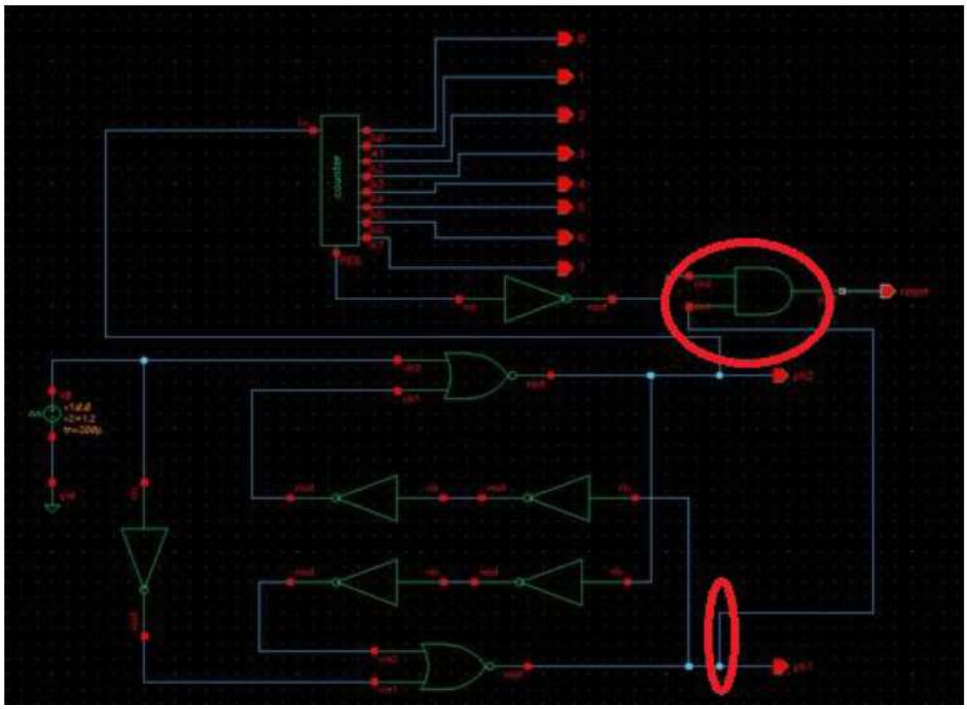

Fig. 32: Solution to this Problem

Conclusion

This technical report demonstrated a design an 8-bit switched-capacitor incremental ADC in UMC 0.13µm CMOS. The design requirements are Supply voltage: 1.2V, Reference voltage (Vref): 1V, Resolution: 8 bits, Output data rate: 100 samples per second and Input voltage range: 0V to 1V. Furthermore, the determine the architecture of incremental A/D converter involved in fuzzy theory. The output waveforms of the clock generator plot with a proper time scale. In the result, we showed the digital outputs and plot the waveforms at the comparator's output for three DC input values: One near 0V, one near Vref/2 and one near Vref. The exact DC values give the offset and gain errors of proposed circuit, supported by simulation results. We also simulated the DNL and INL using a histogram method and give the plots of the DNL and INL of the ADC for all output.

Finally, we conclude the case report with a discussion of results (comparison, problems, solution, possible improvements, etc.).

Acknowledgment

We thanks the lecturers and tutors for Analog Circuit Designof MSC in Electrionic Enginering, The Chinese University of Hong Kong.

Author's Contributions

Zehong Cao, Ze Chen and Xinlong Cai: Conducted the circuit design.
Ze Chen: Wrote this manuscript.

Ethics

This article is original and contains unpublished material. The corresponding author confirms that all of the other authors have read and approved the manuscript and there are no ethical issues involved.

References

A/DCHT, 2012. A/D converter histogram test.

Acharyu, A., P. Hurst and S. Lewis, 2003. Thermal noise from switches in a switched-capacitor gain stage. Proceedings of the Southwest Symposium on Mixed-Signal Design, Feb.25-25, IEEE Xplore Press, Las Vegas, NV, USA, pp: 121-126. DOI: 10.1109/SSMSD.2003.1190410

Chen, Y. and K.P. Pun, 2012. A 0.5-V 90-dB SNDR 102 dB-SFDR audio-band continuous-time delta-sigma modulator. Analog Integr. Circ. Sig. Process, 71: 159-169. DOI: 10.1007/s10470-011-9741-3

Ho, M.H., Y.Q. Ai, T.C.P. Chau, S.C.L. Yuen and C.S. Choy *et al*., 2012. Architecture and design flow for a highly efficient structured ASIC. IEEE Trans. VLSI Syst., 21: 424-433. DOI: 10.1109/TVLSI.2012.2190478

Li, B. and K.P. Pun, 2014. A high image-rejection SC quadrature bandpass DSM for low-IF receivers. IEEE Trans. Circuits Syst., 61: 92-105. DOI: 10.1109/TCSI.2013.2268588

Li, B., L. Sun, C.T. Ko, A.K.Y. Wong and K.P. Pun, 2014. A high-linearity capacitance-to-digital converter suppressing charge errors from bottom-plate switches. IEEE Trans. Circuits Syst., 61: 1928-1941. DOI: 10.1109/TCSI.2014.2298285

PCA/DC, 2012 Parameter calculations A/D converter.

Pun, K.P., S. Lei and B. Li, 2013. Unit capacitor array based SAR ADC. Microelectron. Reliability, 53: 505-508. DOI: 10.1016/j.microrel.2012.09.012

Sun, L., A. Wong, B. Li, W.T. Ng and K.P. Pun, 2015. A charge recycling SAR ADC with a LSB-down switching scheme. IEEE Trans. Circuits Syst., 62: 356-365. DOI: 10.1109/TCSI.2014.2363517

Sun, L., C.T. Ko and K.P. Pun, 2014a. Optimizing the stage resolution in pipelined SAR ADCs for high-speed high-resolution applications. IEEE Trans. Circuits Syst., 61: 476-480. DOI: 10.1109/TCSII.2014.2327372

Sun, L., K.P. Pun and W.T. Ng, 2014b. Capacitive digital-to-analogue converters with least significant bit down in differential successive approximation register ADCs. IET J. Eng., 2014: 45-48. DOI: 10.1049/joe.2013.0219

Tang, X. and K.P. Pun, 2014. New fully-differential amplifier-less pipelined ADC with wide power scalability and ERBW. Analog Integrated Circuits Signal Process., 80: 427-435. DOI: 10.1007/s10470-014-0358-1

Tang, X., C.T. Ko and K.P. Pun, 2012. A charge-pump and comparator based power-efficient pipelined ADC technique. Microelectron. J., 43: 182-188. DOI: 10.1016/j.mejo.2011.12.009

Tang, X., W.T. Ng and K.P. Pun, 2015. A resistor-based sub-1V CMOS smart temperature sensor for VLSI thermal management. IEEE Trans. Very Large Scale Integrat. Syst., 23: 1651-1660. DOI: 10.1109/TVLSI.2014.2348328