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Low Transition Test Pattern Generator Architecture for Built-in-Self-Test

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Abstract: Problem statement: In Built-In Self-Test (BIST), test patterns are generated and applied to the Circuit-Under-Test (CUT) by on-chip hardware; minimizing hardware overhead is a major concern of BIST implementation. In pseudorandom BIST architectures, the test patterns are generated in random nature by linear feedback shift registers. This normally requires more number of test patterns for testing the architectures which need long test time. **Approach:** This study presents a novel test pattern generation technique called Low-Transition Generalized Linear Feedback Shift Register (LT-GLFSR) with bipartite (half fixed) and bit insertion (either 0 or 1) techniques. Intermediate patterns (by bipartite and bit (either 0 or 1) insertion technique) inserted in between consecutive test patterns generated by GLFSR which is enabled by a non overlapping clock scheme. This process is performed by finite state machine generate sequence of control signals. Low-Transition Generalized Linear Feedback Shift Registers (LT-GLFSR), are used in a circuit under test to reduce the average and peak power during transitions. LT-GLFSR patterns high degree of randomness and correlation between consecutive patterns. LT-GLFSR does not depend on circuit under test and hence it is used for both BIST and scan-based BIST architectures. **Results and Conclusion:** Simulation results prove that this technique has reduction in power consumption and high fault coverage with minimum number of test patterns. The results also show that it reduces the peak and average power consumption during test for ISCAS'89 bench mark circuits.

Key words: As Linear Feedback Shift Registers (LFSRs), Circuit-Under-Test (CUT), Design-For-Testability (DFT), Automatic Test Equipment (ATE), Built-In Self-Test (BIST)

INTRODUCTION

Importance of testing in Integrated Circuit is to improve the quality in chip functionality that is applicable for both commercially and privately produced products. The impact of testing affects areas of manufacturing as well as those involved in design. Given this range of design involvement, how to go about best achieving a high level of confidence in IC operation is a major concern. The desire to attain a high quality level must be tempered with the cost and time involved in this process. These two design considerations are at constant odds. It is with both goals in mind (effectiveness and cost/time) that Built-In-Self Test (BIST) has become a major design consideration in Design-For-Testability (DFT) methods. BIST is beneficial in many ways. First, it can reduce dependency on external Automatic Test Equipment (ATE) because it is large, vendor specific logic, non-scalable and expensive equipment. This aspect impacts the cost/time constraint because the ATE will be utilized less by the current design. In addition, BIST can provide high speed, in system testing of the Circuit-Under-Test (CUT) (Pradhan *et al*., 2005). This is crucial to the quality component of testing. Chatterjee and Pradhan (2003) discussed that stored pattern BIST, requires high hardware overhead due to memory devices is in need to store pre computed test patterns, pseudorandom BIST, where test patterns are generated by pseudorandom pattern generators such as Linear Feedback Shift Registers (LFSRs) and Cellular Automata (CA), required very little hardware overhead. However, achieving high fault coverage for CUTs that contain many Random Pattern Resistant Faults (RPRFs) only with (pseudo) random patterns generated by an LFSR or CA often requires unacceptably long test sequences thereby resulting in prohibitively long test time. In general, the dissipation of power of a system in

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test mode is higher than in normal mode operation. Power increases during testing (Chatterjee, 1997) because of high switching activity, parallel testing of nodes, power Due to additional load (DFT) and decrease of correlation(Chen and Hsiao, 2003) among patterns. This extra power consumption due to switching transitions (average or peak) can cause problems like instantaneous power surge that leads to damage of circuits (CUT), formation of hot spots and difficulty in verification. Solutions that are commonly applied to relieve the extravagant power problem during test include reducing frequency and test scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. The aim of BIST is to detect faulty components in a system by means of the test logic that is incorporated in the chip. It has many advantages such as at-speed testing and reduced need of expensive external Automatic Test Equipment (ATE). In BIST, a Linear Feedback Shift Register (LFSR) generates Pseudorandom test patterns are primary inputs for a combinational circuit or scan chain inputs for a sequential circuit (Girard *et al*., 2001) has given. On the observation side, a Multiple Input Signature Register (MISR) compact test set responses received from primary outputs or scan chain outputs (Zorian, 1993). In, BIST-based structures are very vulnerable to high-power consumption during test. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern; hence the power dissipation is more in test mode.

Prior work: Pradhan *et al*. (1999) presented a GLFSR, a combination of LFSR and cellular arrays, that can be defined over a higher order Galois field GF (2^{δ}), $\delta>1$. GLFSR's yield a new structure when the feedback polynomial is primitive and when ($\delta>1$) it is termed as MLFSR.

Corno *et al*. (2000) proposed a cellular automata algorithm for test pattern generation in combinational logic circuits. This maximizes the possible fault coverage and minimizes length of the test vector sequences. Also it requires minimum hardware.

A low power/energy BIST architecture based on modified clock scheme test pattern generator was discussed (Girard *et al*., 2001), it has been proposed that an n bit LFSR is divided into two n/2 bit length LFSRs. The fault coverage and test time are the same as those achieved in conventional BIST scheme.

Wang and Gupta (2002) presented a dual speed LFSR for BIST test pattern generation. The architecture comprises of a slow speed LFSR and a normal speed LFSR for test pattern generation. Slow speed LFSR is clocked by dual clocked flip-flop, this increases the area overhead than normal speed LFSR.

Pradhan and Liu (2005) have discussed an effective pattern generator should generate patterns with high degree of randomness and should have efficient area implementation. GLFSR provide a better random distribution of the patterns and potentially lesser dependencies at the output. EGLFSR is an enhanced GLFSR, using more XOR gate in a test pattern generator which achieves a better performance.

Nourani *et al*. (2008) deals with a low power test pattern generation for BIST applications. It exploits Low Transition LFSR which is a combination of conventional LFSR and insertion of intermediate patterns (bipartite and random Insertion Technique) between sequences of patterns generated by LFSR that can be implemented by modified clock scheme.

Sakthivel and Kumar (2012), A low transition generalized linear feed back shift regiter based test pattern generator for BIST architecture. LT-GLFSR (bipartite) consists of GLFSR with bipartite technique.It is called as insertion of two intermediate patterns between two consecutive patterns generated by GLFSR. It has more transition in between each bits of the pattern generated and (Sakthivel and Kumar, 2011) an adjacent bits of test patterns generated by LT-GLFSR is swapped by using multiplexer is called as bit swapping low transition generalized linear feedback shift register.In this method, generated patterns has greater degree of randomness and high corelation between consecutive patterns but it has slightly high transitions in sequence of patterns generated. Generally, power consumption is with respect to number of transition between cosecutive patterns, if transition is more, power consumption is more in test pattern generator and CUT. By increasing the enable signals to activate the GLFSR, to reduce the number of transitions. In proposed method, LT-GLFSR can activated by four non-overlaping enable signals. This enable signal is to activate test pattern generator partly and remaining in idle when period of test pattern generation.

Proposed work: This study presents a new test pattern generator for low-power BIST (LT-GLFSR), which can be employed for combinational and sequential (scan-based) architectures. The proposed design is composed of GLFSR and intermediate patterns insertion technique (Bipartite and bit insertion technique) that can be implemented by modified clock scheme codes generated by Finite State Machine (FSM). FSM generates sequence of codes (en1en2sel1sel2) which are given by 1011, 0010, 0111, 0001. Enable signals (en1en2) are used to enable part of the GLFSR and selector signals (sel1sel2) are used to select either GLFSR output or bit insertion circuit output. Intermediate patterns are in terms of GLFSR output and bit insertion technique output. The proposed technique

increases the correlation in two dimensions: (1) the vertical dimension between consecutive test patterns (Hamming Distance) and (2) the horizontal dimension between adjacent bits of a pattern sent to a scan chain. Reducing the switching activity in turn results in reducing the average and peak power consumption (Pradhan *et al*., 2005). The GLFSR (Pradhan and Gupta, 1991) structure is modified into it automatically inserts three intermediate patterns between its original pairs genearated. The intermediate patterns are carefully chosen using bipartite and bit insertion techniques (Nourani *et al*., 2008) and impose minimal time to achieve desired fault coverage. Insertion of Intermediate pattern is achieved based on non overlapping clock scheme (Girard *et al*., 2001). The Galois Field (GF) of GLFSR (3, 4) (Wen-Rong and Shu-Zong, 2009) is divided into two parts, it is enabled by non overlapping clock schemes. The randomness of the patterns generated by LT-GLFSR has been shown to be better than LFSR and GLFSR. The favorable features of LT-GLFSR in terms of performance, fault coverage and power consumption are verified using the ISCAS benchmarks circuits.

MATERIALS AND METHODS

GLFSR frame work: The structure of GLFSR is illustrated in Fig. 1. The Circuit Under Test (CUT) is assumed to have δ outputs which form the inputs to that GLFSR to be used as the signature analyzer (Pradhan and Chatterjee, 1999; Matsushima *et al*., 1997). The inputs and outputs are considered δ bit binary numbers, interpreted as elements over GF (2^{δ}).The GLFSR, designed over GF (2^{δ}), has all its elements belonging to GF (2^{δ}). Multipliers, adders and storage elements are designed using conventional binary elements. The feedback polynomial is represented in Eq. 1 as:

$$\Phi(x) = x^{m} + \Phi_{m-1}x^{m-1} + ... + \Phi_{1}x + \Phi_{0} \quad (1)$$

The GLFSR has m stages, D_0, D_1...D_{m-1} each stage has δ storage cells. Each shifts δ bits from one stage to the next. The feedback from the $D_{m-1}{}^{th}$ stage consists of δ bits and is sent to all the stages. The coefficients of the polynomial Φ_i are over GF (2^{δ}) and define the feedback connections.

The GLFSR when used to generate patterns for circuit under test of n inputs can have m stages, each element belonging to GF(2^{δ}) where (m × δ) is equal to n. A non zero seed is loaded into the GLFSR and is clocked automatically to generate the test patterns. In this study GLFSR with (δ>1) and (m>1) are used, where all possible $2^{m\delta}$ test patterns are generated. The feedback polynomial is a primitive polynomial of degree m over GF(2^{δ}). The polynomial from (Wen-Rong and Shu-Zong, 2009) is described as in Eq. 2:

$$\Phi(x) = (x+\beta^{2^{\delta 0}})(x+\beta^{2^{\delta 1}})(x+\beta^{2^{\delta m-1}}) \quad (2)$$

where, β is the primitive element of GF ($2^{m\times\delta}$) and Construct Primitive Polynomial of degree m over GF(2^{δ}) using (equation.2) coefficients Φ_0, Φ_1.., Φ_{m-1} as powers of β, the primitive element of GF($2^{m\times\delta}$). Let δ = 3,m = 4, (GF(3,4)) The primitive polynomial GF(2^{12}) and GF(2^3) are denoted by β and α respectively in Eq. 3:

$$\Phi(x) = (x+\beta)(x+\beta^{8})(x+\beta^{64})(x+\beta^{512}) \quad (3)$$

Expanding the polynomial as in Eq. 4:

$$\Phi(x) = \left(x^{4} + \beta^{1755}x^{3} + \beta^{2340}x^{2} + \beta^{585}\right) \quad (4)$$

Solving the roots α of primitive polynomial p(x):

$$p(x) = x^{3} + x + 1 \quad (5)$$

Is the primitive polynomial of GF(2^3), in GF(2^{12}), β^{1755} becomes an element which corresponds to a primitive element of GF(2^3), α. Substituting the corresponding values, the feedback polynomial is as in Eq. 6:

$$\Phi(x) = x^{4} + ax^{3} + a^{6}x^{2} + a^{5} \quad (6)$$

The element α, α^5 and α^6 are represented as x, x^5 and x^6 respectively in the polynomial form. The four Storage element of the GLFSR are represented as D_1 = $a_5 x^2 + a_4x + a_3$, $D_2 = a_g x^2 + a_7x + a_6$ and $D_3 = a_{11} x^2 + a_{10}x + a_9$ respectively. At each cycle, the values that are to be fed back into the storage elements are given by polynomials:

$$\left(a_{11}x^{2} + a_{10}x + a_{9}\right)\Phi_{0}$$
$$\left(a_{11}x^{2} + a_{10}x + a_{9}\right)\Phi_{1} + a_{2}x^{2} + a_{1}xa_{0}$$
$$(a_{11}x^{2} + a_{10}x + a_{9})\Phi_{2} + a_{5}x^{2} + a_{4}x +$$
$$a_{3}\left(a_{11}x^{2} + a_{10}x + a_{9}\right)\Phi_{3} + a_{3}x^{2} + a_{7}x + a_{6}$$

With the above explanations the generalize GLFSR in Fig. 1 is applied for GLFSR (3,4) defined over GF(2^3) and its structure is given in Fig. 2.

Table 1 shows the first 15 states of the GLFSR (3, 4) with the initial seed "1111, 1111, 1111" and the GLFSR (1, 12), which is a 12 stages LFSR as a comparison.

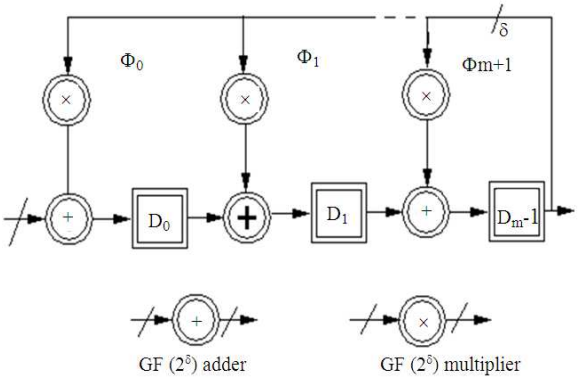


Fig. 1: The generalized GLFSR

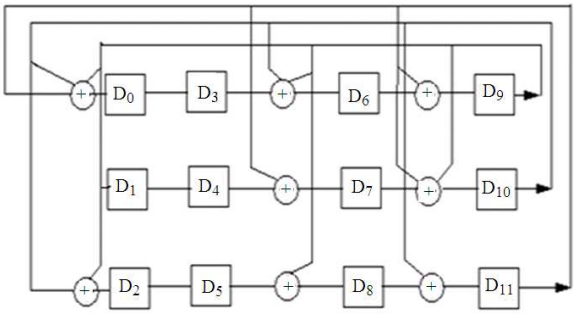


Fig. 2: Structure of GLFSR (3, 4)

Table 1: First 15 states of the GLFSR and LFSR

GLFSR (3,4)	LFSR (n = 12)
1111, 1111, 1111	1111, 1111, 1111
1101, 1110, 0010	0111, 1111, 1111
1011, 1001, 1101	0011, 1111, 1111
0111, 0100, 1111	0001, 1111, 1111
1100, 1111, 0100	1000, 1111, 1111
1111, 1011, 0100	0100, 0111, 1111
1111, 1101, 1100	0010, 0011, 1111
1111, 1101, 0001	1001, 0001, 1111
1001, 1110, 1100	0100, 1000, 1111
1111, 0001, 0111	1010, 0100, 0111
1101, 1111, 1111	0101, 0010, 0 011
1101, 1010, 0010	1010, 1001, 0001
1011, 1001, 0101	0101, 0100, 1000
0111, 0100, 1110	1010, 1010, 0100
0100, 1110, 0010	0101, 0101, 0010
1010, 1011, 1101	1010,1010,1001

Bipartite (Half-Fixed) and Bit Insertion Technique (Intermediate Patterns Insertion Technique): The implementation of a GLFSR is to improve in some design features, such as power, during test. However, such a modification may change the order of patterns or insert new pattern that affect the overall randomness. Insertion of Intermediate patterns between T^i and T^{i+1} of GLFSR by bipartite and bit insertion technique (Nourani *et al*., 2008).

Bipartite (half fixed) technique: The maximum number of transitions will be n when T^i and T^{i+1} are complements of each other. One strategy, used in (Zhang *et al*., 1999) to reduce number of transitions to maximum of n/2, is to insert a pattern T^{i1}, half of which is identical to T^i and T^{i+1}. This Bipartite (half-fixed) strategy is shown symbolically in Fig. 3a.

Bit Insertion Technique (0 or 1): Bit Insertion Technique (either 0 or 1) is called randomly insert a value in positions:

$$t_j^{i1} = \begin{cases} t_j^{i1} \text{ if } t_j^i = t_j^{i+1} \\ \text{Iif } t_j^i \neq t_j^{i+1} \end{cases} \quad (7)$$

where, $t_j^i \neq t_j^{i+1}$, Briefly:

Bit insertion technique symbolically represented as shown in Fig. 3b. The cells (indicated b and $\bar{b}$) show those bit positions where $t_j^i \neq t_j^{i+1}$. We insert a random bit (shown as I in T^{i1}) if the corresponding bits in T^i and T^{i+1} are not equal (0 and 1) is shown in equation.6. Note that, inserted bits are uniformly distributed over the length of the test vector.

Implementation of LT-GLFSR (with Bipartite and Bit Insertion Technique) Technique: Implementation of proposed method, the GLFSR combine with bipartite and bit insertion technique for low-power BIST. It is called LT-GLFSR. The proposed method generates three intermediate patterns (T^{i1}, T^{i2} and T^{i3}) between two consecutive random patterns (T^i and T^{i+1}) generated by GLFSR which is enabled by non overlapping clock schemes.LT-GLFSR provides more power reduction compared to LT-GLFSR (bipartite), conventional GLFSR and LFSR techniques. An intermediate pattern inserted by this technique has high randomness with low transitions can do as good as patterns generated by GLFSR in terms of fault detection and High fault coverage.

In bipartite technique, each half of T^{i1} is filled with half of T^i and T^{i+1} is shown in Eq. 7:

$$T^{i1} = \left\{ t_1^i, \ldots t_2^i, t_{\frac{n}{2+1}}^{\frac{i+1}{}}, \ldots, t_n^{i+1} \right\} \quad (8)$$

In previous study, GLFSR with bipartite technique, GLFSR is divided into two parts by applying two complementary (non-overlapping) enable signals (En1 and En2). First part of GLFSR is including flip-flops are D_0,D_1,D_3, D_4, D_6, D_7, D_9 and D_{10}.. Second part is D_2, D_5, D_8 and D_{11}. In other words, one of the two parts of GLFSR is working, when other part is in idle mode. GLFSR including flip-flops with two different enable signals is shown in Fig. 4a.

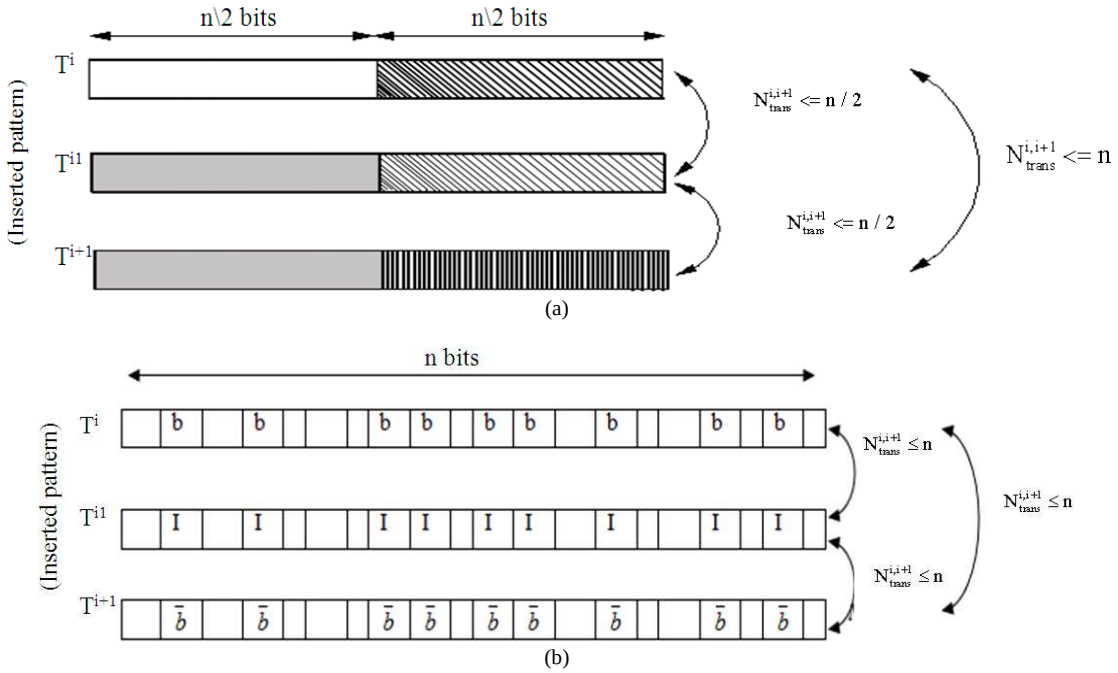
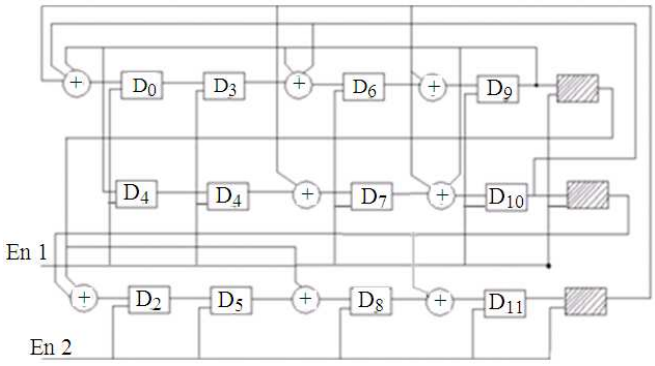


Fig. 3b: (a) Patterns insertion based on bipartite strategy (b) Patterns insertion based on Bit insertion strateg

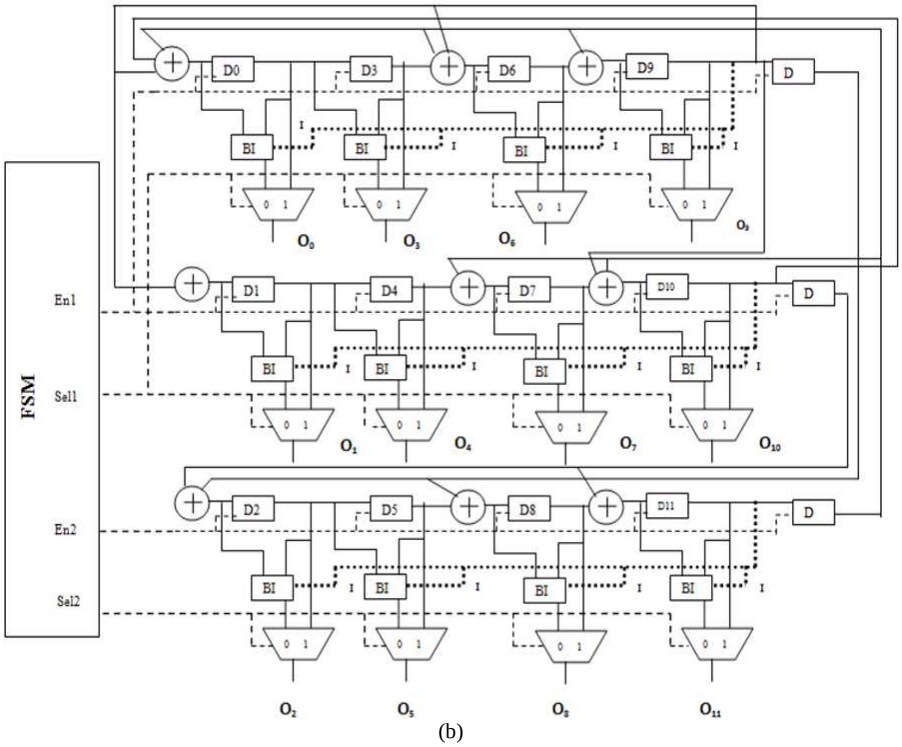
Table 2: Test Patterns for first 20 states

Test pattern	LFSR	LT-GLFSR bipartite	LT-GLFSR bipartite and bit insertions
1	111111111111	111111111111	111111111111
2	011111111111	011100100110	111111111110
3	001111111111	101111011100	111111111100
4	100111111111	111101100000	111111111000
5	001001111111	101110011000	111111110000
6	000100111111	101001111000	111111100001
7	000010011111	000110111101	111111000011
8	100001001111	111011111010	111111000111
9	110000100111	000010111100	111110000111
10	011000010011	110011111000	111110001111
11	001100001001	010010111000	111100001111
12	000110000100	000101100000	111100011110
13	000011000010	001011000000	111000011110
14	000001100001	110110000101	111000111100
15	000000110000	001111000111	110000111100
16	000000011000	101000011011	110000111001
17	000000001100	000101111011	100000111001
18	100000000110	001011100011	100001110010
19	110000000011	110111000011	000011110010
20	111000000001	011011011011	000011100100
21	011100000000	010110100110	000111100100

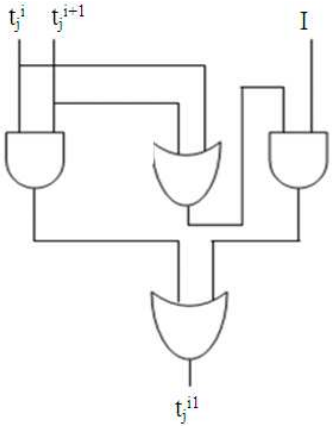
In proposed method, GLFSR with bipartite and bit insertion technique has four different enable signals is as shown in Fig. 4b. It has four non overlapping enable signals are En1, En2, Sel1 and Sel2.Generally, En1 and En2 are to activate GLFSR with bipartite technique as shown in Fig. 4d and Sel2 and Sel2 are to activate GLFSR with bit insertion technique as shown in Fig. 4e by bit insertion circuit as shown in Fig. 4c. Sequence of enable signals generated by finite state machine are given as 1011,0010,0111 and 0001.En1 and En2 are enable a part of GLFSR. Sel1 and Sel2 are selector signals of multiplexers and Hence, its select output of either GLFSR or Bit insertion circuit with respect to enable and selector signals. The first part of GLFSR is working and second part is idle, When En1En2Sel1Sel2 =1011. The second part works and first part is in idle, when En1En2Sel1Sel2 = 0111. Idle mode part has to provide output as present state (stored value). Output of test pattern generator is in terms of part of GLFSR output in idle mode and remaining part is output of bit insertion circuit, when En1En2Sel1Sel2 = 0001 and 0010.Purpose of additional Flip-Flops (shaded flip-flops (D)) are added to the LT- GLFSR architecture is to store the n^{th},$(n-1)^{th}$ and $(n-2)^{th}$ bits of GLFSR. Initially, to store the $(n-1)^{th}$ and $(n-2)^{th}$ bits of GLFSR , when En1En2 = 10 and send $(n-2)^{th}$ bit value into the XOR gate of D2 and D8 flip-flop and $(n-1)^{th}$ bit value into the XOR gate of D2 and D11 flip-flop, when second part becomes active, that is En1En2 = 01.Finally, to store the n^{th} bit of GLFSR, when En1En2 = 01 and send its value into the XOR gate of D0,D7 and D10 flip-flop when the first part becomes active En1En2 = 10.



(a)

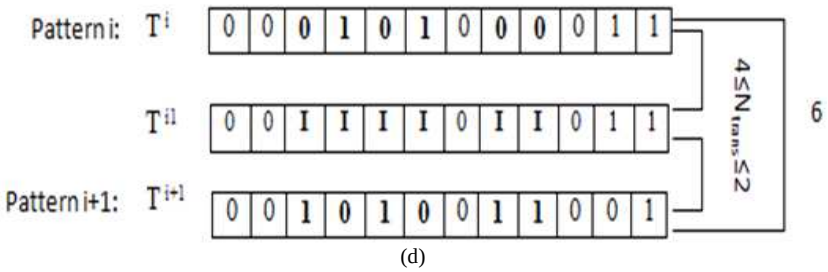


(b)

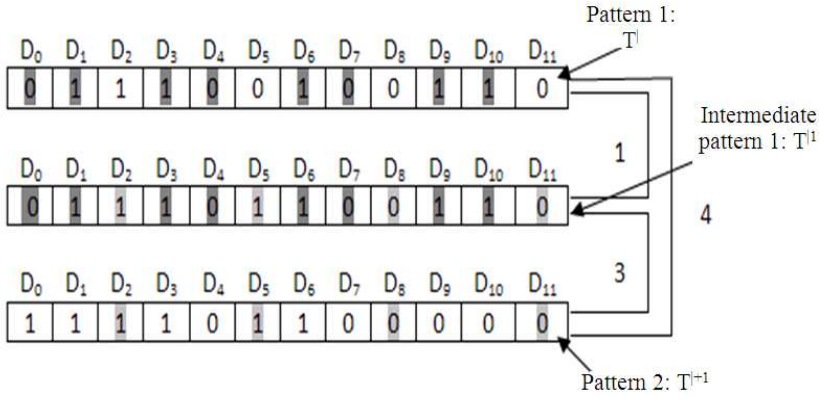


t_j^i	t_j^{i-1}	t_j^{i1}
0	0	0
1	0	1
0	1	I
1	0	I

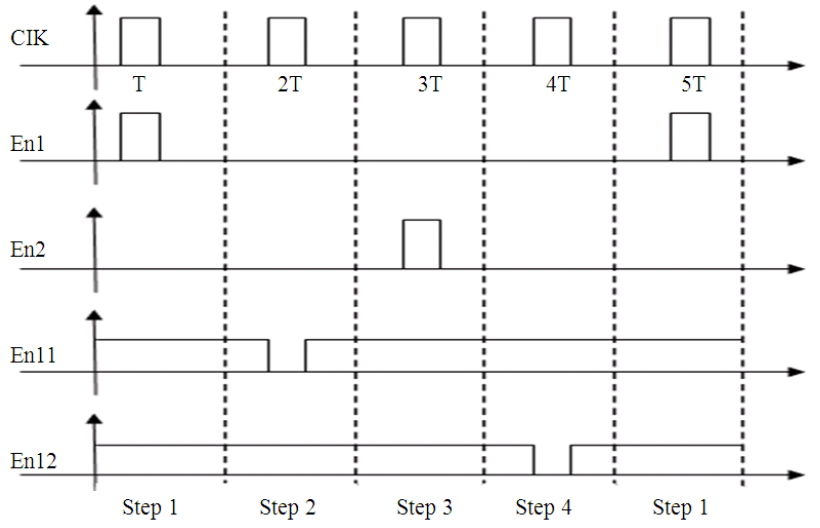
(c)



(d)



(e)



(f)

Fig. 4: (a) Architecture of LT- GLFSR with Bipartite Technique) (b) Architecture of LT- GLFSR with Bipartite and Bit insertion Technique (c) An BI Circuit (d) Bit Insertions in LT-GLFSR Bipartite Technique (e) Bit Insertions in LT-GLFSR Bipartite Technique (f) Timing diagram of Enable signals

Generally, the output of LT-GLFSR is based on enable and selector signals. Note carefully that the new (shaded (D)) flip-flop does not change the characteristic function of GLFSR. The GLFSR's operation is effectively split into two parts and it is enabled by the four different enable signals as shown in Fig. 4f. This method is similar to the Modified clock scheme LFSR (Girard *et al*., 2001). They were used two n/2 length LFSRs with two different non-overlapping clock signals which increases the area overhead. Insertion of Intermediate patterns T^{i1}, T^{i2} and T^{i3} between two consecutive patterns generated by GLFSR (3, 4) is T^i and T^{i+1}.

One part of the LT-GLFSR flip-flops are clocked in each cycle, but in conventional LFSR and GLFSR flip-flops are clocked at the same time in each clock cycle, thus its power consumption is much higher than LT-GLFSR. The power consumed by LFSR, GLFSR, LT-GLFSR (bipartite and LT-GLFSR (bipartite and bit insertion) with ISCAS bench mark circuits are tabulated as shown in Table 3 and 4.

The following steps are involved to insert the intermediate patterns in between two consecutive patterns.

Step 1: $en_1en_2 = 10$, $sel_1sel_2 = 11(1011)$.

The first part (D_0, D_1, D_3, D_4, D_6, D_7, D_9 and D_{10}) of GLFSR is active and the second Part (D_2, D_5, D_8 and D_{11}) is in idle mode. Selecting $sel_1sel_2 = 11$, both parts of GLFSR are sent to the outputs (O_1 to O_n). In this condition first part (D_0,D_1,D_3,D_4,D_6,D_7,D_9 and D_{10}) of GLFSR are send to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as next state and no bit change in second part (D_2,D_5,D_8 and D_{11}) of GLFSR are send to the outputs (O_2,O_5,O_8 and O_{11}) as its present state (Stored value). In this case, T^i is generated.
Step 1 to generate T^{i+1}.

Step 2: $en_1en_2 = 00$, $sel_1sel_2 = 10(0010)$.

The both parts of GLFSR are in idle mode. The first Part of GLFSR is sent to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as its present state (stored value) but the bit insertion circuit inserts a bit (0 or 1) to the outputs (O_2,O_5,O_8 and O_{11}). T^{i1} is generated.

Step 3: $en_1en_2 = 01$, $sel_1sel_2 = 11(0111)$.

The first part of GLFSR is in idle mode. The second part of GLFSR is active. In this condition first part (D_0,D_1,D_3,D_4,D_6,D_7,D_9 and D_{10}) of GLFSR is send to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as present state and second part (D_2,D_5,D_8 and D_{11}) of GLFSR is send to the outputs (O_2,O_5,O_8 and O_{11}) as its next state T^{i2} is generated.

Step 4: $en_1en_2 = 00$, $sel_1sel_2 = 01(0001)$.

Both Parts of GLFSR are in idle mode. The second part of GLFSR is send to the Outputs (O_2, O5, O8 and O_{11}) as its Present state. Bit insertion circuit insert a bit (0 or 1) into the outputs (O_0, O_1, O_3, O_4, O_6, O_7, O_9 and O_{10}). T^{i3} is generated.

Step 5: The process continues by going through

Table 3: Transition fault detected in S298

Pattern generation	Number of test pattern	Pattern reduction (%)	Power (mW)
LFSR	53	--	45.56
GLFSR	17	32.09	25.98
LT-GLFSR (Bipartite)	12	22.67	21.23
LT-GLFSR (Bipartite and Bit insertion)	8	15.09	18.23

Table 4: Transition fault detected in S526

Pattern generation	Number of test Pattern	Pattern reduction (%)	Power (mW)
LFSR	567	--	58.9
GLFSR	234	41.26	39.7
LT-GLFSR (Bipartite)	197	34.74	31.6
LT-GLFSR (Bipartite and Bit insertion)	102	17.98	20.12

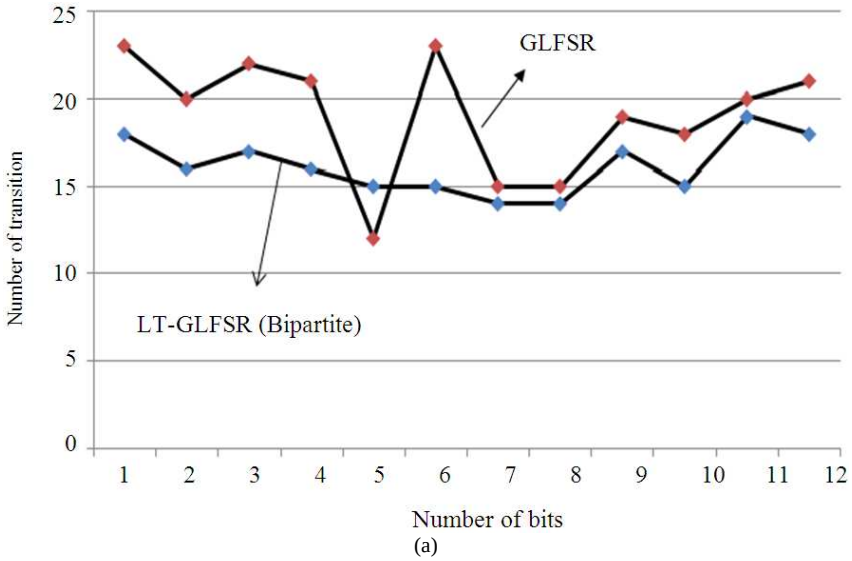
RESULTS

The test patterns generated by LFSR, LT-GLFSR (Bipartite) and LT-GLFSR (Bipartite and Bit Insertion) as shown in Table 2 are used for verifying the ISCAS85 benchmark circuits S298 and S526. Simulation and synthesis are done in Xilinx 13 and power analysis is done using Power analyzer.

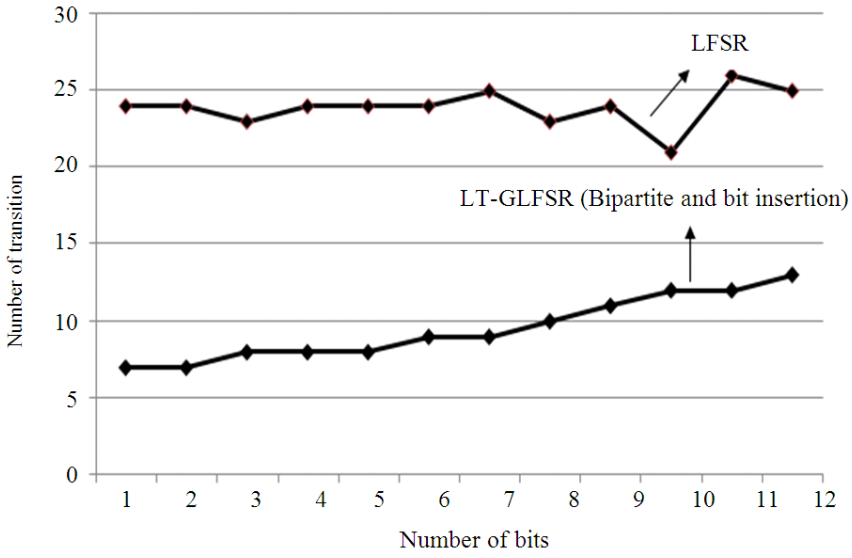
The results in Table 3 and 4, are the test patterns for fault coverage and the reduction in the number of test patterns. Power analysis is carried out with the maximum, minimum and typical input test vectors for stuck-at faults and transition faults of sequential Circuits (CUT).

Programming of the design is done in VHDL and simulation of the design is carried out using MODEL SIM 6.5. Table 2 shows the first 20 states of the LT-GLFSR (3, 4) with the initial seed "1111, 1111, 1111" and which are 20 stages of LFSR and LT-GLFSR (bipartite) for comparison.

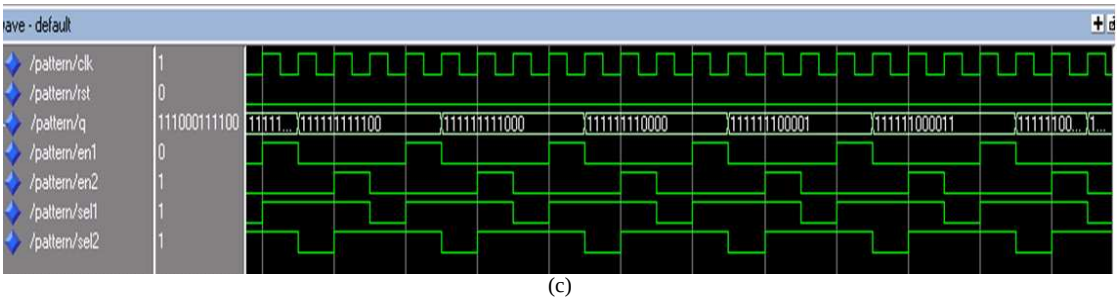
Figure 5a shows the distribution of the number of transitions in each Bit of the pattern generated using GLFSR and LT-GLFSR (bipartite) for 50 patterns. Transitions in each bit of the patterns generated LT-GLFSR (bipartite) is varies in between 14-19 transitions. It has comparatively less number of transitions with patterns generated by GLFSR. Figure 5b shows the distribution of the number of transitions in each bit of the pattern generated using LFSR and LT-GLFSR (bipartite and bit insertion) and also It shows number of transitions in patterns generated by proposed method is very less when compared with LFSR, GLFSR and LT-GLFSR (bipartite).Hence, test patterns generated by LT-GLFSR (bipartite and bit insertion) has very less transitions (varies from 7-14) and consumes very low power compare with other methods. This test patterns reduces switching transitions in test pattern generator as well as circuit under test.



(a)



(b)



(c)

Fig. 5: (a) Distribution of the number of transitions in each Bit of the pattern generated using GLFSR and LT-GLFSR(bipartite) for 50 patterns (b) Distribution of the number of transitions in each Bit of the pattern generated using LFSR and LT-GLFSR (bipartite and bit insertion) for 50 patterns (c) LT-GLFSR (Bipartite and Bit Insertion) Test pattern generator

DISCUSSION

Test patterns are generated by LFSR, LT-GLFSR (bipartite) and LT-GLFSR (bipartite and bit insertion) and the analysis of randomness or closeness among the bit patterns are done. From the analysis the test patterns generated by LT-GLFSR (bipartite and bit insertion) has significantly greater degree of randomness, resulting in improved fault coverage when compared to standard LFSR and GLFSR. GLFSR is modified by means of clocking such that during a clock pulse one part is in idle mode and other part in active mode. This modification is known as LT-GLFSR which reduces transitions in test pattern generation and increases the correlation between and within the patterns by inserting intermediate patterns. From the discussed three methods, the LT GLFSR has less number of test patterns required for high fault coverage with high degree of closeness, randomness and low power consumption for the CUT.

CONCLUSION

An effective low-power pseudorandom test pattern generator, LT-GLFSR (bipartite and bit insertion) is proposed in this study. Power consumption of LT-GLFSR is reduced due to the Bipartite and bit insertion technique. Only half of the LT-GLFSR flip-flops are clocked in each cycle. LT-GLFSR's provide for greater randomness than standard LFSR and GLFSR, which have the potential to detect most stuck-at and transition faults for CUT with a fraction of patterns. This will be significance for the faults detection for ISCAS circuits with a minimum number of input test patterns. The switching activity in the CUT and scan chains, their power consumption are reduced by increasing the correlation between patterns and also within each pattern. This is achieved with almost no increase in test length to hit the target fault coverage.

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