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Design of Transmitter for CDM Based 2×2 Multiple Input Multiple Output Channel Sounder for Multipath Delay Measurement

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Abstract: Problem statement: Multiple Input Multiple Output (MIMO) wireless communication system is an innovative solution to improve the bandwidth efficiency by exploiting multipath-richness of the propagation environment. The degree of multipath-richness of the channel will determine the capacity gain attainable by MIMO deployment. **Approach:** Therefore, it is very important to have accurate knowledge of the propagation environment/radio channel before MIMO implement. The radio channel behavior can be anticipated by channel measurement or channel sounding. Code Division Multiplexing (CDM) is one of the channel sounding techniques that allow accurate measurement at the cost of hardware complexity. CDM based channel sounder, requires code with excellent auto-correlation and cross-correlation properties which generally difficult to be achieved simultaneously. **Results:** In this study, an efficient transmitter for CDM-based 2×2 MIMO channel sounding technique with Loosely Synchronous (LS) codes is designed. Simulation results shows that the channel sounding scheme using LS codes gives very good performance for measuring 2×2 MIMO channel behavior. The BPSK transmitter is designed using MATLAB, Verilog and Xilinx system generator blocks. **Conclusion:** The whole design is simulated as a single ISE project by using ModelSim simulation tool and compiled using ISE 9.2. However the proposed design of transmitter using LS code of length 8190 bits can measure multipath delay of minimum 0.13 μs and maximum 520 μs.

Key words: MIMO, transmitter, channel sounder, CDM, multipath delay

INTRODUCTION

Multiplexing multicarrier communications have become very important for the future communications networks. Numerous researches on antenna technology are ongoing both in industry and academia to provide reliable communication systems (Numan *et al*., 2010). Recently the demand for both higher data rates and more reliable wireless communications in severe multipath fading is rapidly increasing. In real environment accurate knowledge of the propagation channel is required to process MIMO receiving systems. Thus, the accuracy of MIMO channel measurement is an important issue in many aspects like simulation, system design and performance analysis. A major research focus in this area has been the use of multiple antennas for transmitting and receiving instead of the traditional single antenna systems. It has been proposed that using multiple transmit and receive antennas and associated coding techniques could increase the performance of wireless communication. So far, there has been a lot of theoretical research but relatively few practical systems have been demonstrated. Knowing the characteristic of the MIMO channel parameters is very important issue to determine performance of the MIMO system.

In order to have a satisfactory channel characterization, the amplitudes, phase shifts and delays associated with each multipath component in the channel model must be determined. In view of the multitude of possible propagation environments, a deterministic modeling of these parameters is not feasible. The characteristics of mobile radio channels lead to the conclusion that their behavior is non-stationary (Ullah *et al*., 2011) and in practice characterization proves extremely difficult unless stationary is assumed over short distances of travel or short intervals of time. Channel sounder allows estimation of the parameters associated with the impulse response of a radio channel, namely the number of multipath components and their associated amplitudes, phases and delays. In its simplest form a channel sounder can be nothing more than bi-static pulsed radar that transmits a repetitive pulse of width

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T_{bb} seconds and uses a receiver with a wide band pass filter, the received signal is then amplified, detected with an envelope detector, acquired and stored. The minimum resolvable delay between multipath components is equal to the probing pulse width T_{bb}, while the repetition rate T_{REP} determines the maximum unambiguous excess delay that can be resolved (Ullah *et al*., 2008; 2009a; 2009b; Ibrahimy *et al*., 2009) the pulse repetition rate must be fast enough to allow observation of the time-varying response of individual propagation paths, while the time interval between pulses must be long enough to ensure that all multipath signals have decayed between successive pulses. This type of system gives an immediate measurement of the square of the channel impulse response convolved with the probing pulse; however it is subject to interference and noise due to the wide band pass filter required for multipath delay resolution; besides, the transmitted signal must have a high peak-to-mean power ratio to provide adequate detection of weak multipath components. No information about the phases of the multipath components can be obtained in this type of system due to the use of an envelope detector.

The previous schemes for MIMO channel measurement are to Use Time-Division Multiplexing with Synchronized switching (TDMS) based MIMO channel sounder (Choi *et al*., 2006). Although this technique is cost effective, it has the major drawback that absolute time synchronization and excess time slots are needed. As another approach, Code-Division Multiplexing (CDM) based MIMO channel sounder with low correlation codes was introduced (Choi *et al*., 2006; Islam *et al*., 2009a; 2009b; 2010a; 2010b; 2011; Shakib *et al*., 2010; Tsoulos, 2006). However, it also has disadvantage that dynamic range is limited by the number of transmit antennas due to none-zero correlation values. In this study an efficient transmitter with Loosely Synchronous (LS) code sequence with optimized Interference Free Window (IFW) for CDM based 2×2.

MATERIALS AND METHODS

A BPSK Transmitter with LS Code generator is designed using the Sundance FPGA development boards. The proposed design block diagram and explanation is shown in Fig. 1.

LS code generator: Code-Division Multiplexing (CDM) based MIMO channel sounder with low correlation codes was introduced (Choi *et al*., 2006). Due to the excellent correlation properties of the Loosely Synchronous Code, it can solve the problem caused in TDMA system. In CDM system it is really challenging to have such code sequence with good auto and cross correlation property at the same time.

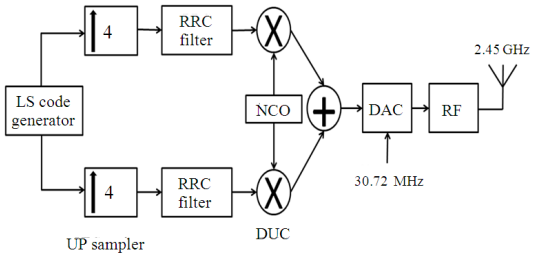

Fig. 1: Block diagram of BPSK transmitter

LS codes are defined as the combination of C and S subsequences, a Golay complementary pair, with zeros inserted to avoid overlapping between the two subsequences. If (C0, S0) and (C1, S1) are both Golay pairs of LS codes (Choi and Hanzo, 2002). As a result of inserted zeros, LS codes have features that aperiodic autocorrelation side lobes and cross-correlations are zero within IFW zone. The main purpose of zeros insertion of the LS codes is to avoid the sequences C0 and C1 overlapping with the sequences S0 and S1. Note that it is also necessary to insert enough guard intervals between sequences with length longer than the maximum delay of the multipath channel.

LS code correlation properties: The definitions and properties of Auto and Cross Correlation Functions (ACF/CCF) of any two codes LS_i and LS_j (Kim *et al*., 2008) are given as (Eq. 1):

$$R_{ij}(\tau)=\sum_{n=0}^{N-1}C_{i,n}C_{j,(n+\tau)\bmod N}+\sum_{n=0}^{N-1}S_{i,n}S_{j,(n+\tau)\bmod N}$$
$$=\begin{cases}2N, & \tau=0,\ i=j\\ 0, & \tau=0,\ i\neq j\\ 0, & 0<|\tau|<W_{ij}\end{cases} \quad (1)$$

Cross correlation properties of two LS code sequence is observed in simulation result. It has also been observed that IFW width increased with code length. If the code lengths increase the IFW width has been increased. To determine the code length, the delay of multipath channel would be considered. The delay spread must be less then IFW to avoid any overlapping. To ensure the interference-resist ability of the system even when the environment is in bad condition, the IFW between LS codes is expected to be as long as possible, so that most of the interferences will fall into the IFW and the system toleration degree against channel deterioration will be high. The IFW length is restricted by the size of the code set. Therefore, it is important to improve the robustness of the system when the LS code set is fixed. LS code generator designed for 8190 bits of codeset and 4000 bits of IFW achieved.

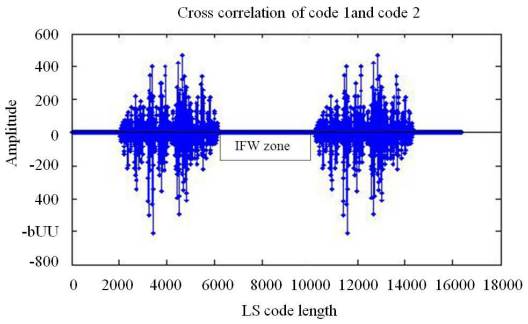

Fig. 2: Simulation result of cross correlation properties of LS codeset

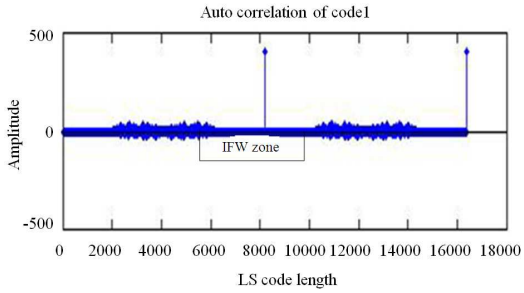

Fig. 3: Simulation result of auto correlation properties of LS codeset

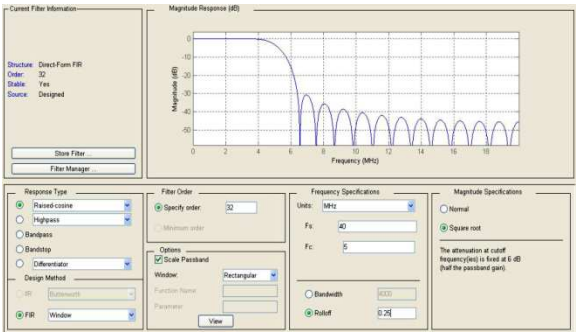

Fig. 4: The response of RRC filter

Figure 2 and 3 shows the cross correlation of code 1 and code and auto correlation of code 1 respectively. Up sampler increases the sampling rate of the signal. In the proposed design the signal up sampled by 4 before pulse shaping.

Root raised cosine filter: The spectrum of a rectangular pulse spans infinite frequency. In such instances, the infinite bandwidth associated with a rectangular pulse is not acceptable. The bandwidth of the rectangular pulse can be limited, however, by forcing it to pass through a filter.

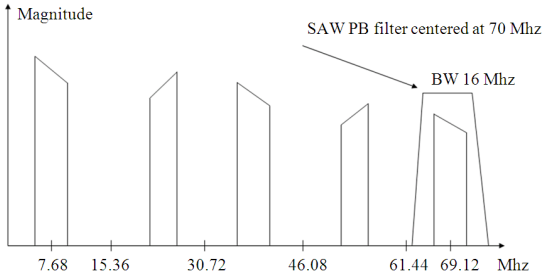

Fig. 5: DAC output spectrum

Table 1: Technical specification of Tx up converter.

Parameter	Value
Linear output power	-20dBm, average
Output power at 1 dB compression	0dBm, minimum
RF frequency range	2400-2500 MHz
Gain control	31dB, in 1dB steps
Gain control accuracy	±2dB Maximum

The act of filtering the pulse causes its shape to change from purely rectangular to a smooth contour without sharp edges. Therefore, the act of filtering rectangular data pulses is often referred to as pulse shaping. System Generator tool provides high-level abstractions that are automatically compiled into a netlist code. Mainly in SIMULINK system generator register, multiplier and constant blocks are used to design RRC filter. System Generator block sets allow us to construct bit-accurate and cycle-accurate models of an FPGA circuit in Simulink.

In the proposed transmitter design, Root Raised Cosine (RRC) filter is designed for the purpose of pulse shaping. Figure 4 shows 32 order response of RRC filter. The netlist generations of the RRC filter to create the Verilog code which is compatible for implementation. The specification of the RRC filter; sampling rate is 7.68 MHz, pulse duration 0.13 μs and the roll off factor is 0.25.

Digital up converter: In the transmitter design the up conversion from 70 MHz IF to the 2.4 GHz RF is done in two stages: The first stage converts the 1st IF to 374 MHz and the second stage converts to the 2.4 GHz RF frequency. Numerically Controlled Oscillator (NCO) is used for up conversion. The specification of up converter is given in Table 1.

Digital to analog converter: DAC converts the 16 bit digital data to analog. The output spectrum of DAC has shown in Fig. 5. The system bandwidth for the transmission is 16 MHz. DAC output image lies within the RF transmitter input bandwidth range centered at 70 MHz. The SAW filter in the RF transmitter will filter out the fundamental and all other images, except the image centered at 69.12 MHz shown in Fig. 5. The RF

Transmitter up-convert 70 MHz signal to 2.45 GHz and transmit it through Antenna. Amplitude of the output spectrum reduces due to DAC sinc effect.

RESULTS

The proposed BPSK transmitter is designed using MATLAB, Verilog and Xilinx system generator blocks. The whole design is simulated as a single ISE project by using ModelSim simulation tool and compiled using ISE 9.2. The ISE project synthesized as top module Tx_lscode_top Module including two submodule lscode1 and lscode2. The ISE project synthesis report, ModelSim simulation result and RTL illustration of top module and sub modules are included in this section.

Figure 6 presents the Register Transfer Level (RTL) schematic of the designed model. In integrated circuit design, RTL description is a way of describing the operation of a synchronous digital circuit. In RTL design, a circuit's behavior is defined in terms of the flow of signals (or transfer of data) between hardware registers and the logical operations performed on those signals.

For the Verilog Simulation, the ISE 9.2 supports the ModelSim XE III 6.4b Waveform entity simulation methods' such as using Vector Waveform File (VWF). The RTL schematic view of Top module of proposed transmitter design is illustrated in Fig. 7. The transmitter top module consists of 2 sub-module lscode1 and lscode2. It has 2 input clk and resetn and 16 bit output data_out_scaled. Figure 7 shows the ModelSim simulation result of the transmitter top module.

Figure 8 shows the RTL schematic view of lscode1 sub-module. The lscode1 sub-module consists of counter and memory. Counter has 3 inputs clk, clken and port adr_q; 12 bits output port_q. Figure 9 shows the ModelSim simulation result of the lscode1 sub-module.

The RTL schematic view of lscode2 sub-module is shown in Fig. 10. The lscode2 sub-module consists of one 14-bit input and one bit output counter, two 14-bit input and one-bit output adder and 1 FDR. Counter has 3 inputs clk, clken and port adr_q; 12 bits output port_q. Figure 11 shows the ModelSim simulation result of the lscode2 sub-module.

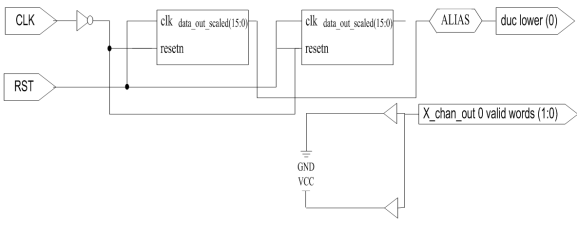

Fig. 6: RTL view of Transmitter top module

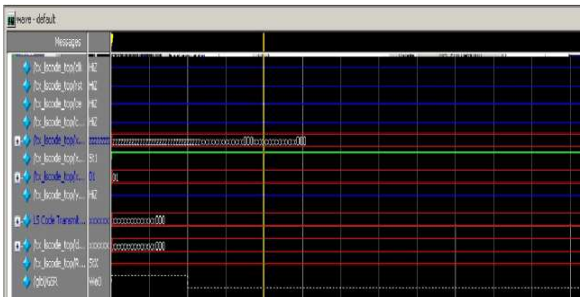

Fig. 7: Simulation result of Tx_lscode_top Module

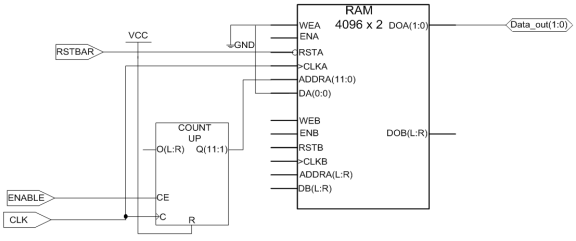

Fig. 8: RTL view of lscode1 sub-module

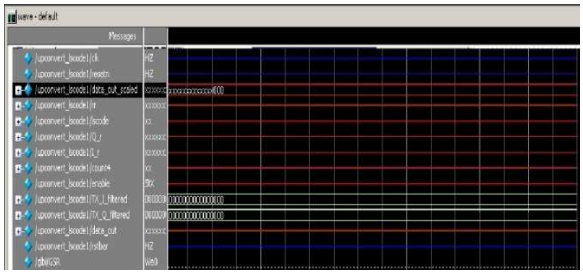

Fig. 9: Simulation result of lscode1 Sub-Module

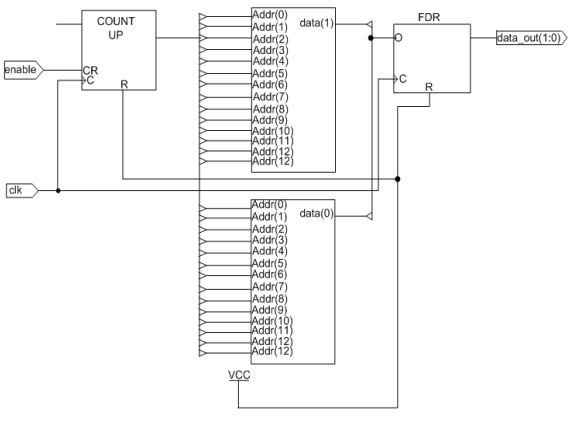

Fig. 10: RTL view of lscode2 sub-module.

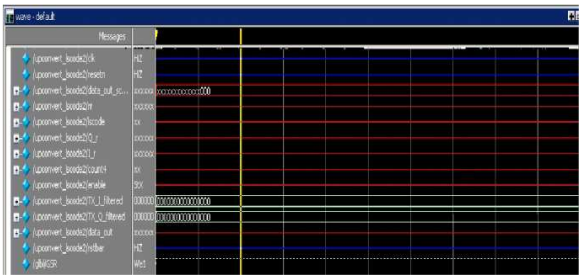

Fig. 11: Simulation result of lscode2 Sub-Module

DISCUSSION

Initially, MATLAB has been used, to design the LS code generator and investigate the correlation properties. After required codeset generated with excellent correlation properties, Xilinx system generator blocks used to design the Root Raised Cosine filter for pulse shaping purpose. The proposed design of transmitter was coded in Verilog, compiled and synthesized in ISE 9.2. For Verilog modeling and implementation, the algorithm has to be thought of as a structural, behavioral and physical version of the algorithm. The components of FPGA, input output and device utilization are shown in the summary report.

CONCLUSION

A BPSK Transmitter for 2×2 CDM based channel sounder has been successfully designed, tested and synthesized by using MATLAB, Xilinx ISE and ModelSIM. The necessary code sequence with excellent auto and cross correlation properties also investigated from LS code. The expected correlation properties of LS code are optimized. Two LS code sequences with same code length are chosen as sounding sequence. From two 8190 bits of code sequences with simulated and the length of IFW are 4000 bits. According to the length of IFW the implemented system can measure minimum 1bit duration and maximum 4000 bit duration. After successfully designed the BPSK transmitter it synthesized and verified. The proposed system can measure the delay of minimum 0.13 μs and maximum 520 μs.

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