

Field Programmable Gate Array-Based Pulse-Width Modulation for Single Phase Active Power Filter

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Abstract: Problem statement: The design and implementation of a sinusoidal Pulse-Width Modulation (PWM) generator for a single-phase hybrid power filter is presented. **Approach:** The PWM was developed in an Altera® Flex 10 K Field Programmable Gate Array (FPGA) and the modulation index was selected by calculating the DC bus voltage of the active filter through a digital controller, by Proportional-Integral-Derivative (PID) technique. **Results:** Experiment results showed the proposed active power filter topology to be capable of compensating the load current and the voltage harmonic, up to IEC limit. **Conclusion:** The implemented PWM generator using an FPGA required less memory usage while providing flexible PWM patterns whether same phase, lagging, or leading, the reference voltage signal.

Key words: Active power filter, PWM, FPGA, power quality

INTRODUCTION

Pulse width modulation techniques have been intensively researched in the past few years. Methods, of various concept and performance, have been developed and described. Their design implementation depends on application type, power level, semiconductor devices used in the power converter, performance and cost criteria, all determining the PWM method.

Two classes of PWM techniques have been identified: optimal PWM and carrier PWM. The optimal PWM technique for producing switching pattern is based on the optimization of specific performance criteria^[1]. In this case, the switching patterns are calculated a priori for given operating conditions and are then stored in memory (look-up tables) for use in real time. Higher gain, from over-modulation, is possible when compared with the conventional PWM scheme. However, considerable computational effort of solving nonlinear equations to derive the switching angles, the large memory required to store the information for various modulation indexes and the relatively sophisticated control to allow smooth transient pattern changes, are considered to be serious practical difficulties^[2].

Most analogue circuits implementing PWM control schemes are based on “natural” sampled switching strategies. More recently, a switching strategy

proposed, referred to as “regular sampling”, is considered to have a number of advantages when implemented digitally. They are immune to noise and are less susceptible to voltage and temperature changes, hence, the digital implementation^[3-6].

Generation of PWM gating signals requires a high sampling rate, for wide-bandwidth performance. Therefore, most computation resources of a microprocessor’s DSP must be devoted to generating PWM signals. Tasks could be segregated by a combination of microprocessor and DSP. A DSP handles the PWM generation while the processor feeds the DSP-required information. Although this method resolves sampling-rate problems, it complicates design^[4].

FPGA is a Programmable Logic Device (PLD), comprising thousands of logic gates. Some of them are combined to form a configurable logic block (CLB). A CLB simplifies high-level circuit design. SRAM or ROM defines software interconnections between logic gates, providing flexible modification of the designed circuit, without altering the hardware. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for complex circuitry and rapid prototyping make it the favorite choice for prototyping an Application Specific Integrated Circuit (ASIC). The advent of FPGA technology has enabled rapid prototyping of the digital system^[7].

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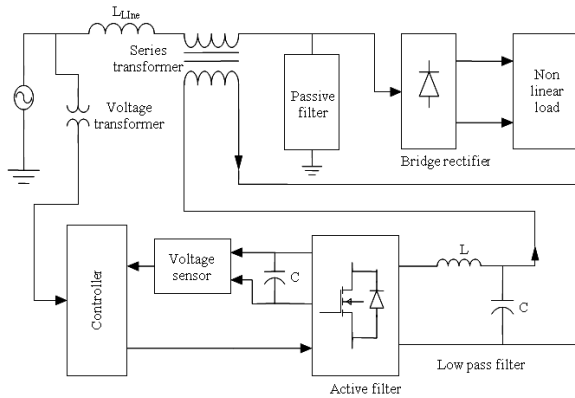


Fig. 1: System configuration of the hybrid active power filter

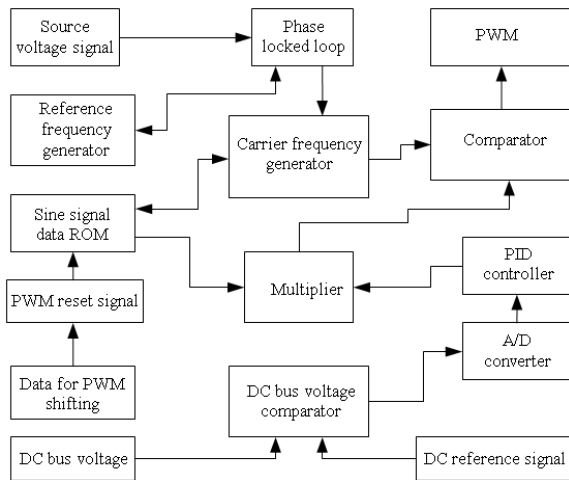


Fig. 2: Block diagram of an active-power-filter control

The active power filter is shown in Fig. 1. In this configuration, the passive filter bypasses the current-harmonic component, according to the designed value of the passive element. The active filter acts as a voltage compensator and a harmonic isolator for the source and for the load. Voltage compensation is by injecting to the line, the in-phase voltage. The harmonic isolation is also by the series compensation, behaving as active impedance, not causing voltage drop for the fundamental component, but forcing the current harmonic component to pass through the passive filter. Thus, the active filter improves both the filtering characteristics of the passive filter and the power factor of the load, by compensating the reactive power required by the load^[6].

Figure 2 is the block diagram of an active-power-filter control. A sinusoidal reference waveform is compared with a triangular carrier waveform, to generate gate signals for the inverter's switches. The amplitude of the modulating wave (the reference waveform) is

obtained by multiplying a fixed amplitude sine wave with the amplitude of a variable processed signal, which, in shape and in amplitude, is the key parameter for the inverter's output voltage control. The processed signal is extracted by comparing with a reference DC value, the DC bus capacitor voltage. The error signal (the difference between the DC bus voltage and the DC reference voltage) is processed by a Proportional, Integral and Derivative, (PID), controller, for stability^[8].

PWM generation: The control of the active filter is digitally implemented in an Altera® FPGA. PWM generation is by logic elements; gates, look-up tables, RAM, flip-flop and programmable interconnected wiring that can, by a technique, be programmed in the field, post-manufacture.

However, the real time generation of a sine wave through FPGA is time consuming. It is, therefore, inappropriate in PWM applications to calculate the modulating wave values, as they are required in 'real time'. An alternative approach is to store the sine values in the look-up table, which is programmed in permanent memory. The sine values are calculated first by this method. Memory requirements, operation efficiency and output waveform accuracy depend on the number of samples defining a sine-wave cycle and their resolution.

For example, if the values are taken at 1° intervals, then the complete modulating cycle is defined by 360 values. The waveform can be defined at a greater number of sample points, but the memory requirements are proportionally increased. Hence, the point when a sample is taken for the modulating process directly corresponds to a value in the look-up table.

A sine voltage equation generates data to store in a ROM for sinusoidal waveform. 49 data is generated for 90° (quarter cycle) of a sine waveform. An up-down counter reads the ROM data. Each counting value determines each data's ROM address. For up-count mode, it counts from 0-48 and for down-count mode, it counts from 47-01. Thus, 96 data represents one complete half cycle. If the previous cycle were considered a positive half cycle, for negative half cycle the same data is counted continuously and separated by digital-AND technique, with 10 ms pulses of 1 and 0s.

Determination of carrier frequency is the first step in design, needing precise calculation of clock frequency. The carrier frequency (f_c) was decided to be 19.2 kHz, the decision based on various factors such as inverter topology, acoustic radiations, type of power-switching devices used and the limitation of peripheral components. High-frequency operation is better than a low-frequency one as harmonic components can be moved to high orders. However, at high frequency, switching stresses and power losses increase^[9].

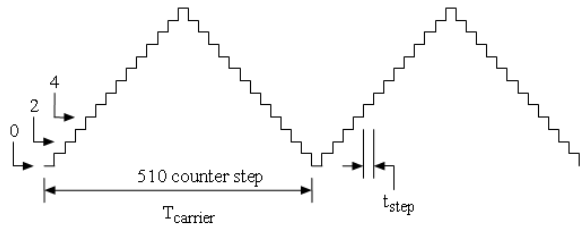


Fig. 3: Pattern of a carrier wave

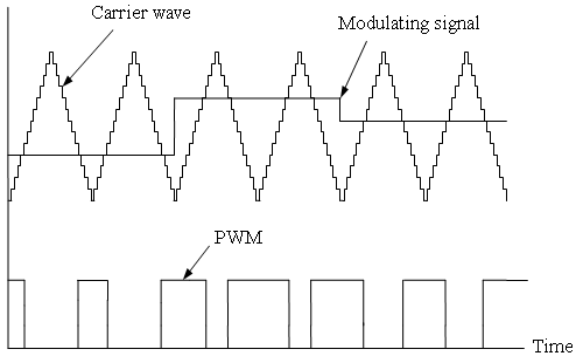


Fig. 4: Pulse generation technique

The carrier frequency relates with the main clock frequency and the up-down counter, through:

$$f_c = \frac{f_{clk}}{(2^n - 1) * 2} \quad (1)$$

Where:

- f_c = The carrier frequency
- f_{clk} = The main clock frequency
- n = The bit size of the up-down counter

Figure 3 shows the developed triangular wave from an up-down counter and some peripheral logic gates. The counter is clocked externally by a clock generated from the phase locked loop circuit. The main clock frequency (f_{clk}) determines the up-down counter's rate of increment or of decrement. When the counter starts up-counting and goes to maximum, some logic gates monitor it and generate a signal for down-counting; similarly, when the counter reaches minimum counting value, the monitoring logics interrupt the counting and the counter changes its counting direction. The process repeats continuously.

Every step of the carrier wave is compared with the multiplied modulating signal from the look-up table as shown in Figure 4. The data for the sine wave is stored in an internal ROM, the address ascending, 49 data for a 90° modulating wave.

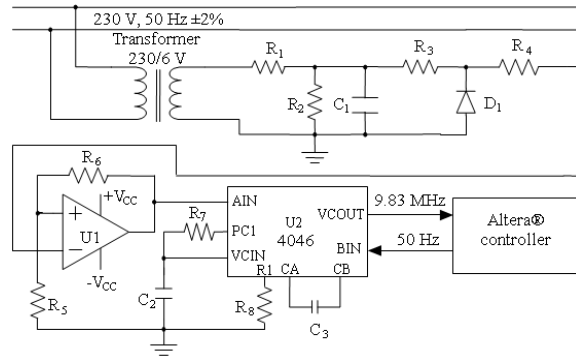


Fig. 5: Phase locked loop

For the data output, taken from the ROM memory, a 7 bit up-down counter is the address for the data in the ROM. The up-counter counts from 0 to 48; when it reaches 48, some logic gates generate an interrupt signal and force the counter to count down from 47-1. The counting time depends on the PWM circuit's design and on the main clock frequency. All 96 data must be synchronized with 192 carrier waves and 10ms operating time, i.e., half cycle (180°) of a sine wave. In its implementation, the counter's clock must be fed with a correct frequency (f_{clk}), for the output designed. Comparison between the carrier and the modulating signal must be done such that when the carrier value is less than, or equal to, the modulating signal, the PWM output level is HIGH and when the carrier value is greater than the modulating value, the PWM output level is LOW.

The comparison is done for every clock pulse in every counting step for the carrier value as well as for the ROM data value. This process is continuous. Every 10 ms, the process repeats. For a four-switch bridge, two sets of out-of-phase pulses are needed. To develop the two sets, the PWM pulse train must be logical-AND, with two sets of continuous 10 ms ON and OFF pulses, exactly opposite in phase, synchronized in-phase with one complete cycle of up-down-counting ROM data. The 10 ms pulses are developed by a frequency divider included in the PWM circuit.

The main clock frequency is generated by a Phase Locked Loop (PLL). 8 bit counter, J-K flip-flops, Adder, Subtractor and all other necessary clocked components, are clocked from the PLL. The main clock frequency is determined from Eq. 1. The clock signal is clocked and synchronized with the 50 Hz ±2% AC mains frequency, by the PLL circuit shown in Fig. 5.

The 9.83 MHz main clock frequency is divided into 50 Hz by the Altera® controller. The 50 Hz feedback frequency is a PLL-chip input that locks with the system frequency. For PWM and other controlling parts,

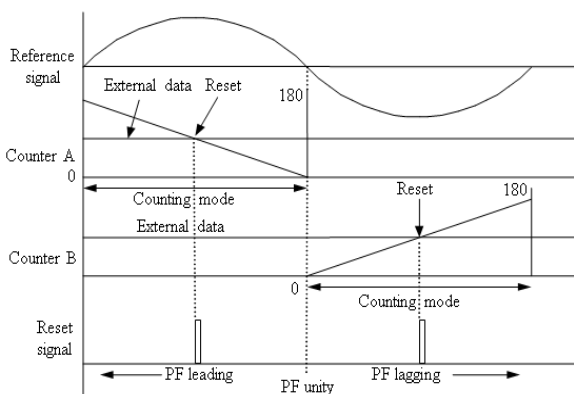


Fig. 6: Phase-shifting realization

clock frequencies are generated by the frequency divider and the counter. A PLL phase-comparator provides a digital error signal that maintains a 90° phase shift between the Voltage Control Oscillator (VCO) centre frequency and the input signal. This error is compensated by using a PWM shifting technique, by count-and-compare where necessary.

Figure 6 shows counters A and B comparing with predefined values their counting value (the phase angle for lagging and leading phase displacements with the system's voltage) and generating a pulse. The pulse resets all the PWM modules, restarting the PWM. If the external data is set to 180° or to 0° in both counters, the PWM pattern is in phase with the reference voltage: Unity power factor.

MATERIALS AND METHODS

The system parameters are shown in Table 1-3. The source voltage wave shape is detected from the source end before the active and passive filter by using isolation amplifier and the source current is detected at the source end before the active and passive filter by using current probe. The voltage-measuring scale is selected from the isolation amplifier setting and oscilloscope voltage scale, for the current, current probe setting and the oscilloscope voltage scale is considered.

The capacitors are selected from the rated value and the inductances are designed. For a higher value of inductance it produces the noise and humming sound, which may produce more loss. A lot of trail tuning makes it possible to adjust the inductance value for the better harmonic compensation.

Table 1: Specification for test system

Passive filters parameters	
Voltage (line-neutral)	110V (rms)
Power source frequency	50 Hz
Source impedance inductance	3 mH
Source impedance resistance	0.8 Ω
Harmonic sources capacitance	200 μF
Harmonic sources resistance	100 Ω

Table 2: passive filter parameters for hybrid active power filter

Passive filters parameters	
Resistance (3rd harmonic)	0.8 Ω
Inductance (3rd harmonic)	18.7 mH
Capacitance (3rd harmonic)	60 μF
Resistance (5th harmonic)	0.6 Ω
Inductance (5th harmonic)	10.6 mH
Capacitance (5th harmonic)	40 μF
Resistance (High pass)	2 Ω
Inductance (High pass)	5 mH
Capacitance (High pass)	30 μF

Table 3: Specification of series connected active power filter

Active power filter specification	
Resistance (AC low pass filter)	0.8 Ω
Inductance (AC low pass filter)	2.5 mH
Capacitance (AC low pass filter)	0.01 μF
Switching frequency	19.2 kHz
Transformer coefficient	0.5
DC side capacitor	400 μF, 400 V

RESULTS

Figure 7 shows the source voltage and the source current before compensation by active and passive filters and Fig. 8 shows the harmonic spectrum of the source current without compensation. Figure 9 shows the source voltage and the source current after compensation by active and passive, filters. Figure 10 shows the harmonic spectrum of the source current of Fig. 9; the THD, 7.78%.

By pulse-shifting technique, the phase displacement between the source voltage and the source current is reduced to almost zero (unity power factor).

The PWM to control the active power filter can be shifted by the count, compare and reset method. Figure 12-14 show the PWM shifting pattern relative to the system voltage.

The effect of PWM-shifting results only in the source current's harmonic content. If the PWM position is 90° leading relative to the system voltage, the source current THD for the inductive load is 6.78%, as Fig. 15 shows. From the harmonic spectrum, the 7th harmonic content is maximal.

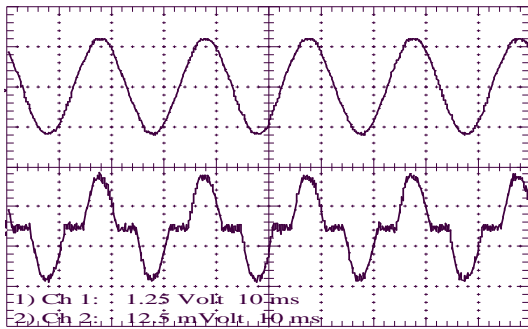


Fig. 7: Source voltage and source current, no compensation

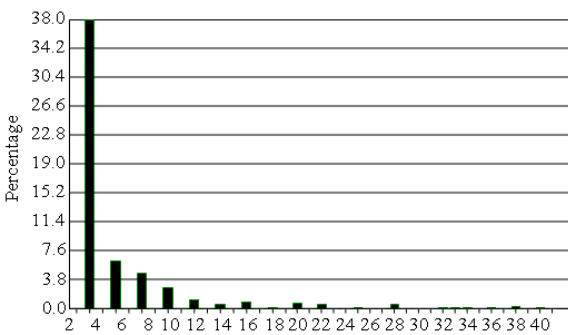


Fig. 8: Harmonic spectrum of the source current of Fig. 7

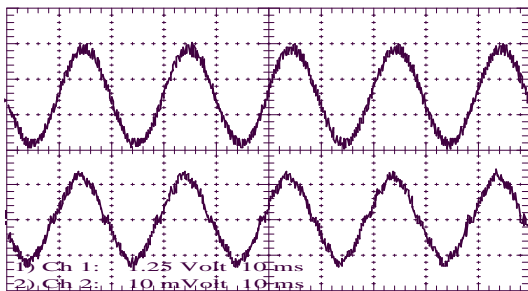


Fig. 9: Source voltage and source current, after compensation

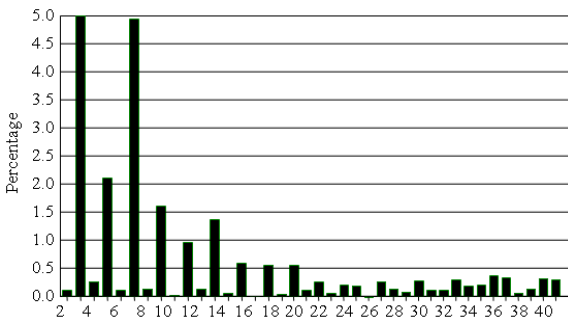


Fig. 10: Harmonic spectrum of source current of Fig. 9

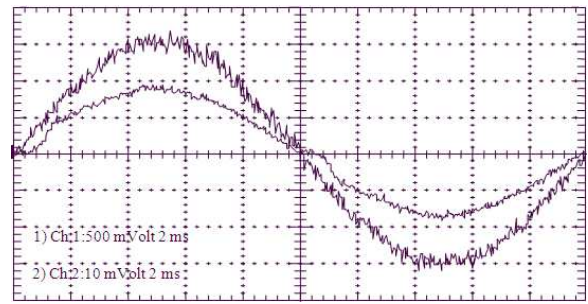


Fig. 11: In-phase pattern of source voltage and source current

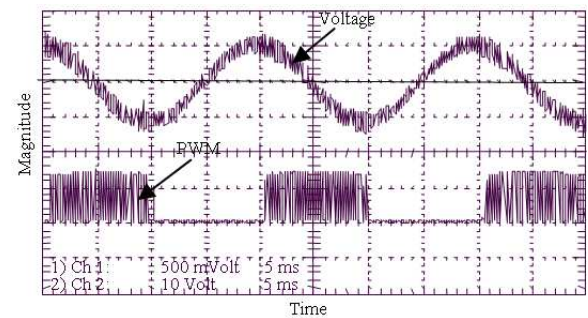


Fig. 12: 90° leading PWM relative to system voltage

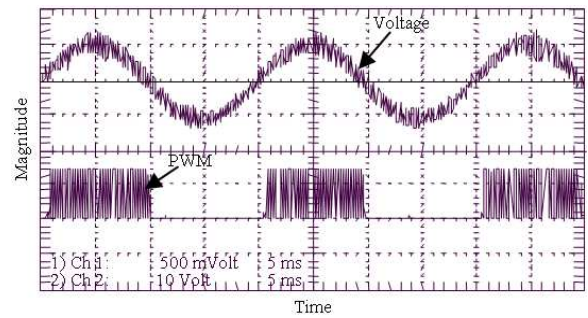


Fig. 13: 0° displaced PWM relative to system voltage

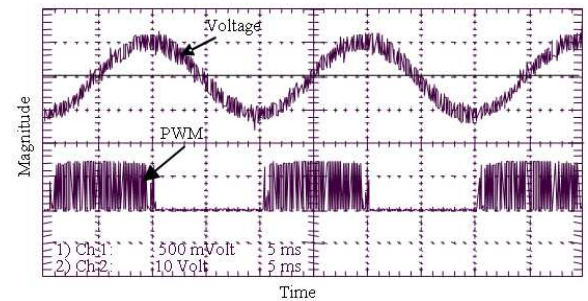


Fig. 14: 90° lagging PWM relative to system voltage

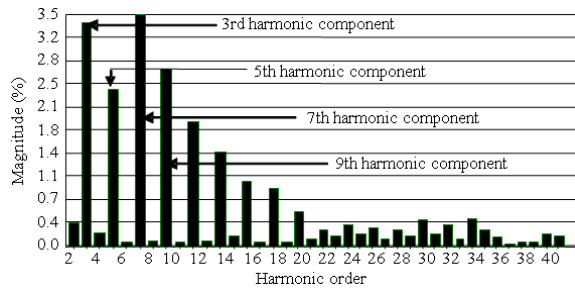


Fig. 15: Source current spectrum for 90° leading PWM

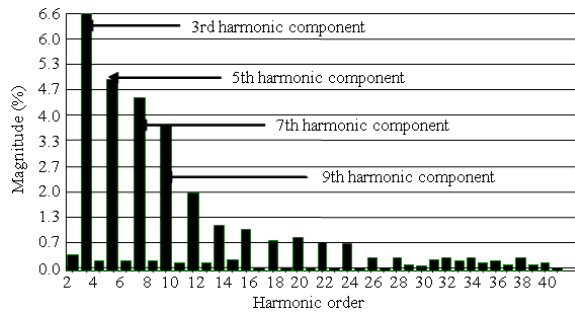


Fig. 16: Source current spectrum for in-phase PWM

Table 4: Total harmonic distortion

	Simulation (%)	Experiment (%)
Before compensation by active and passive filters	32.6	38.99
After compensation by passive filter only	16.0	27.33
After compensation by active and passive filters	6.7	7.78

Figure 16 is the harmonic spectrum of the source current for in-phase PWM; the THD is 10.6%. The 3rd harmonic component is maximum amplitude.

DISCUSSION

The comparison of simulation THD and experiment result THD is shown in Table 4. The THD for source current without compensation is 38.99%. Compensation, by passive filter only, reduced the harmonic by up to 27.33%.

CONCLUSION

The active power filter proposed can compensate for current’s harmonic components and reactive power, also improve load power factor. The PWM design, placed in an Altera® FLEX 10 K FPGA, is flexible in producing PWM patterns, whether same phase, lagging, or leading, the reference voltage signal. The overall

system requires no external memory. Both its hardware and control system satisfy the simulation results and validate the series active and shunt passive, combined filter system.

REFERENCES

1. Agelidis, V.G., P.D. Ziogas and G. Joos, 1996. Dead-band PWM switching patterns. IEEE Trans. Power Elect., 11: 522-531. <http://cat.inist.fr/?aModele=afficheN&cpsidt=3123528>
2. Omar, A.M. and N.A. Rahim, 2003. FPGA-based design of the three-phase synchronous PWM flyback converter. IEE Proc. Elect. Power Appl., 150: 263-268. DOI: 10.1049/ip-epa:20030507
3. Retif, J.M., B. Allard, X. Jorda and A. Perez, 1993. Use of ASIC’s in PWM techniques for power converters. Proceedings of the International Conference on Industrial Electronics, Control and Instrumentation, Nov. 15-19, IEEE Xplore Press, Maui, HI, USA., pp: 683-688. DOI: 10.1109/IECON.1993.338998
4. Tzou, Y.Y., H.J. Hsu, T.S. Kuo, 1996. FPGA based SVPWM control IC for 3-phase PWM inverters. Proceedings of the IEEE 22nd International Conference on Industrial Electronics, Control and Instrumentation, Aug. 5-10, IEEE Xplore Press, Taipei, Taiwan, pp: 138-148. DOI: 10.1109/IECON.1996.570921
5. Bowes, S.R. and A. Midoun, 1985. Suboptimal switching strategies for microprocessor-controlled PWM inverter drives. IEE Proc. B. Elect. Power Appl., 132: 133-148. DOI: 10.1049/ip-b:19850019
6. Rahim, N.A. and Z. Islam, 2004. A single-phase series active power filter design. Proceeding of the International Conference on Electrical, Electronic and Computer Engineering Sept. 2004, IEEE Xplore Press, USA., pp: 926-929. http://ieeexplore.ieee.org/xpls/abs_all.jsp?isnumber=30014&arnumber=1374638&count=297&index=292
7. Itoh, R. and K. Ishizaka, 1991. Three-phase flyback AD-DC converter with sinusoidal supply currents. IEE Proc. B. Elect. Power Appl., 138: 143-151. http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=75445
8. Choe, G.H. and M.H. Park, 1988. New injection method for AC harmonic elimination by active powerfilter. IEEE Trans. Ind. Elect., 35: 141-147. DOI: 10.1109/41.3077
9. Holtz, J., 1992. Pulsewidth modulation-a survey. IEEE Trans. Ind. Elect., 39: 410-420. DOI: 10.1109/41.161472